Flot de conception d'une carte électronique

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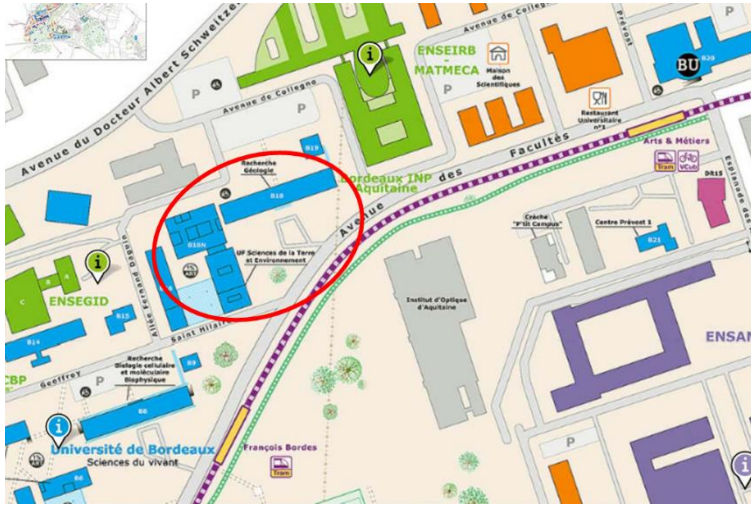
Laboratoire d'Astrophysique de Bordeaux :

- Site historique : Observatoire à Floirac

- Depuis Juillet 2016 : Campus de Talence

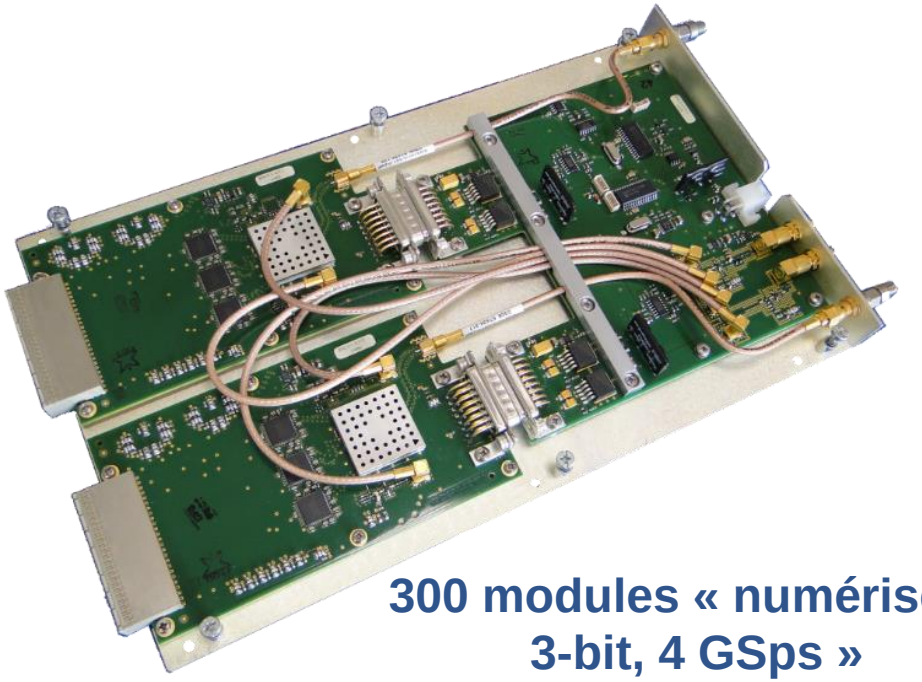


- **Laboratoire d'Astrophysique de Bordeaux :**
  - Etude du milieu interstellaire diffus à la formation des étoiles et des systèmes planétaires,
  - Etude des propriétés atmosphériques et de la surface de planètes,
  - Etude de l'habitabilité et recherche de la vie.

⇒ **Instruments (spectromètre, interféromètre, radar GPR, …)**

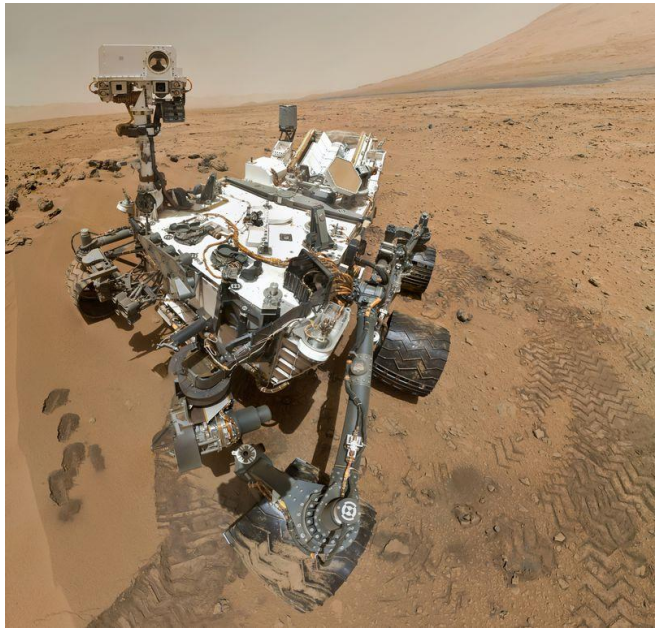
- **Equipe électronique**
  - Permanents : 3 IR, 2 IE, 1 AI, 1 T
  - CDD : 1 IR, 1 IE
  - Système Matériel (jusqu'à 20 GHz) : Cadstar (dessin de cartes), Suite Ansys (RF), Ltspice
  - Système Logiciel : Quartus (Altera), Vivado (Xilinx), Libero (Microsemi), ModelSim (Mentor)
  - Bancs de test : Python, LabView

Interféromètre de 66 antennes au Chili

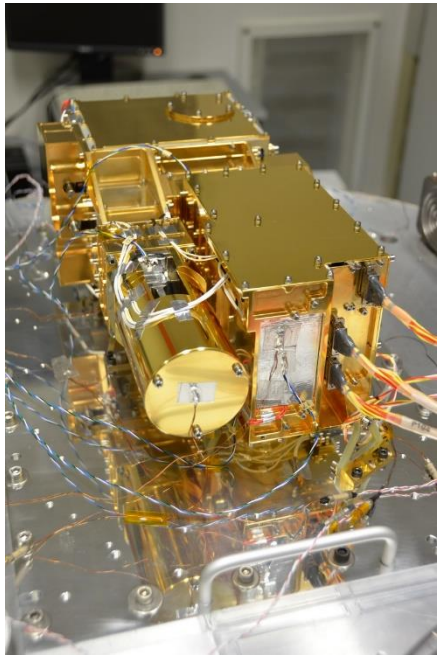


300 modules « numériseur, 3-bit, 4 GSps »

600 cartes « TFB »

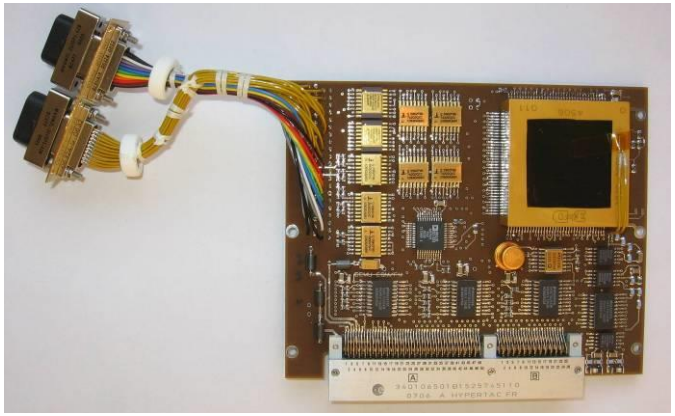


Robot Curiosity



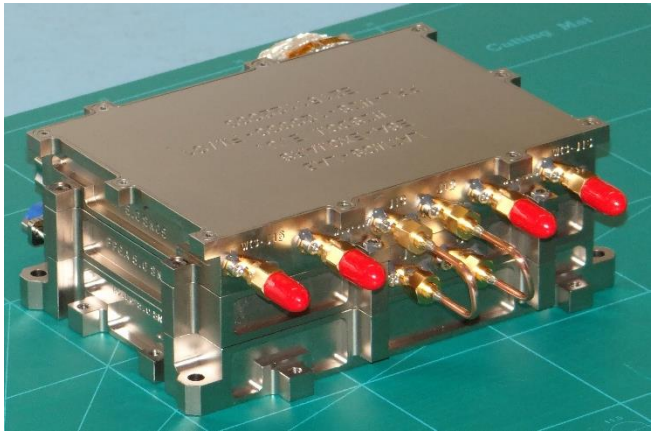
Instrument ChemCAM (Mast Unit)

Jet Propulsion Laboratory
California Institute of Technology

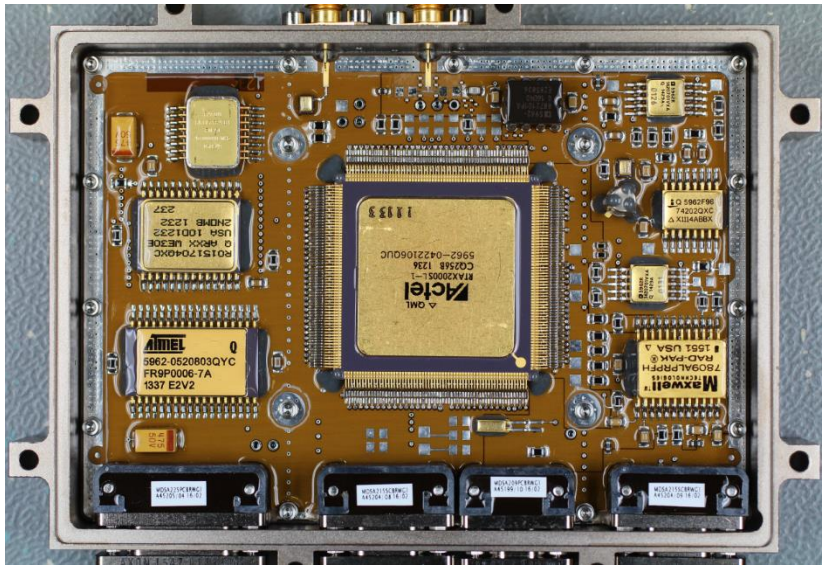


Carte de contrôle

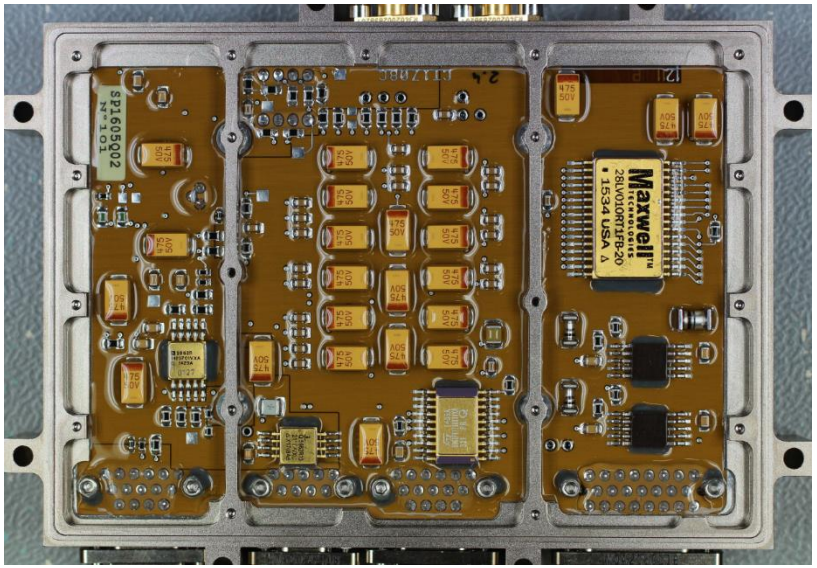
Orbiteur et Robot Exomars



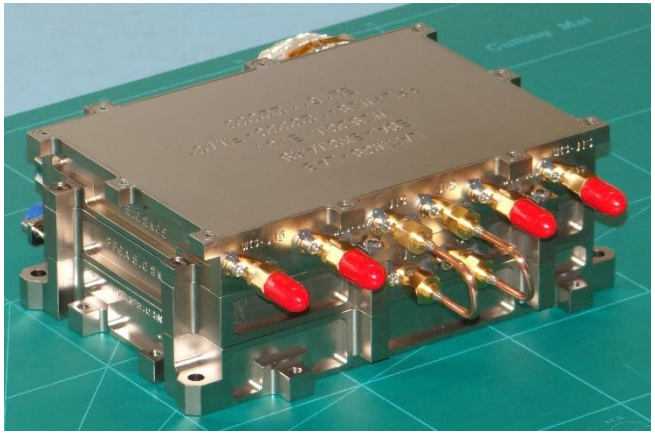
Boîtier électronique du radar GPR



Carte de contrôle

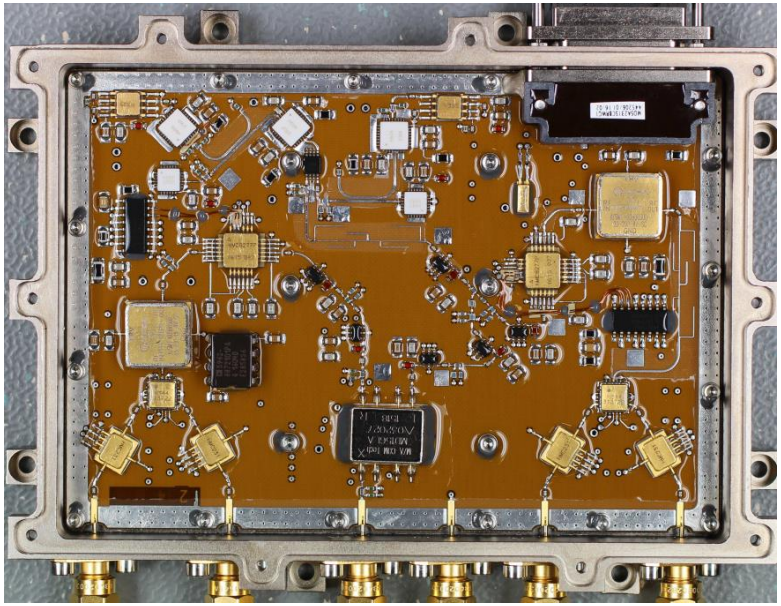


Robot Exomars

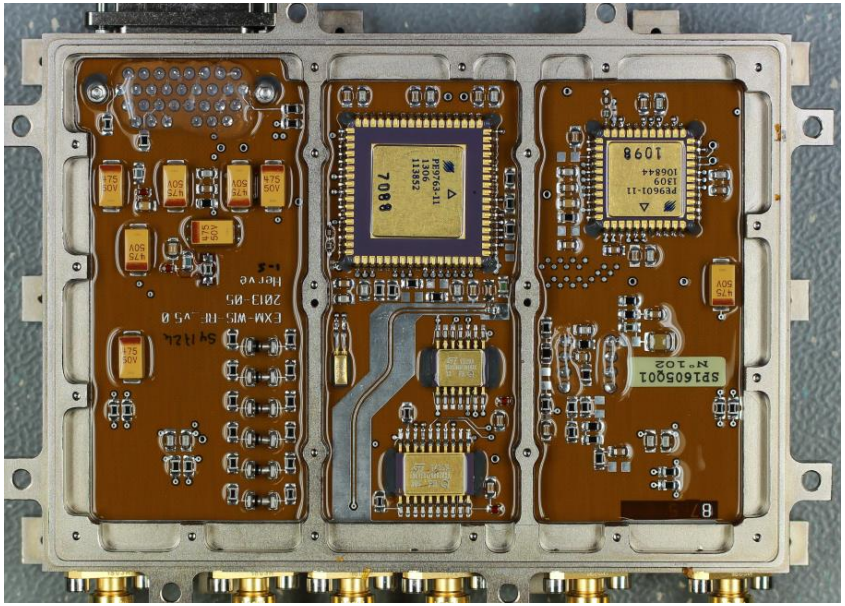


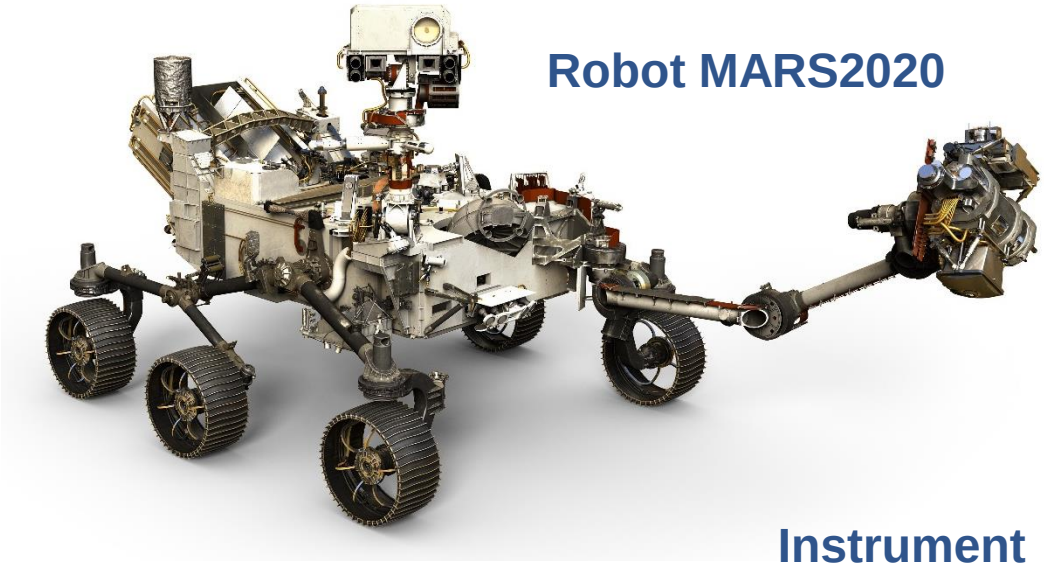
Boîtier électronique du radar GPR

European Space Agency



Carte RF

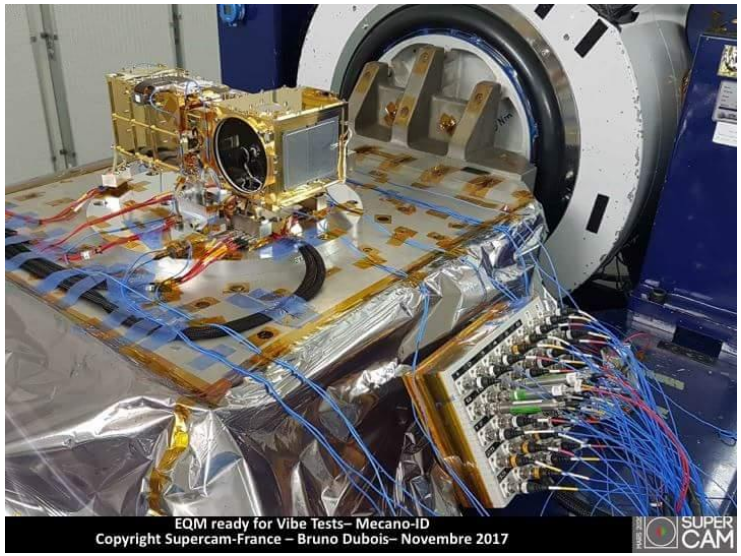


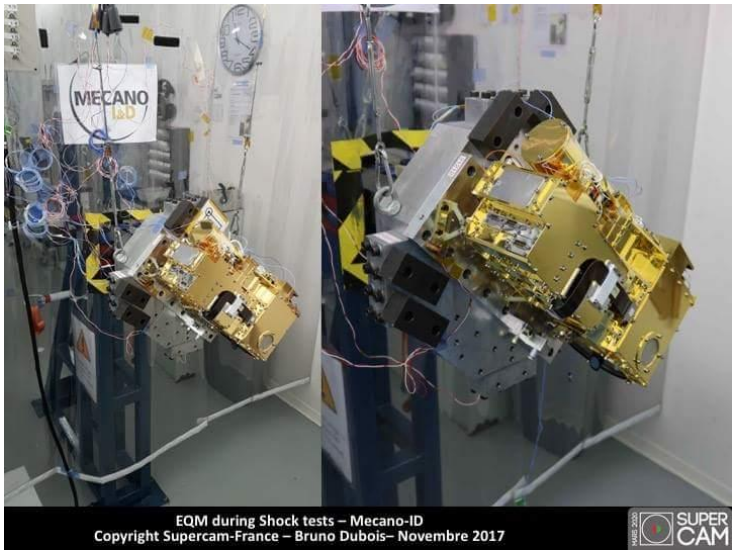


Robot MARS2020

Jet Propulsion Laboratory
California Institute of Technology

Instrument
SuperCAM (Mast Unit)

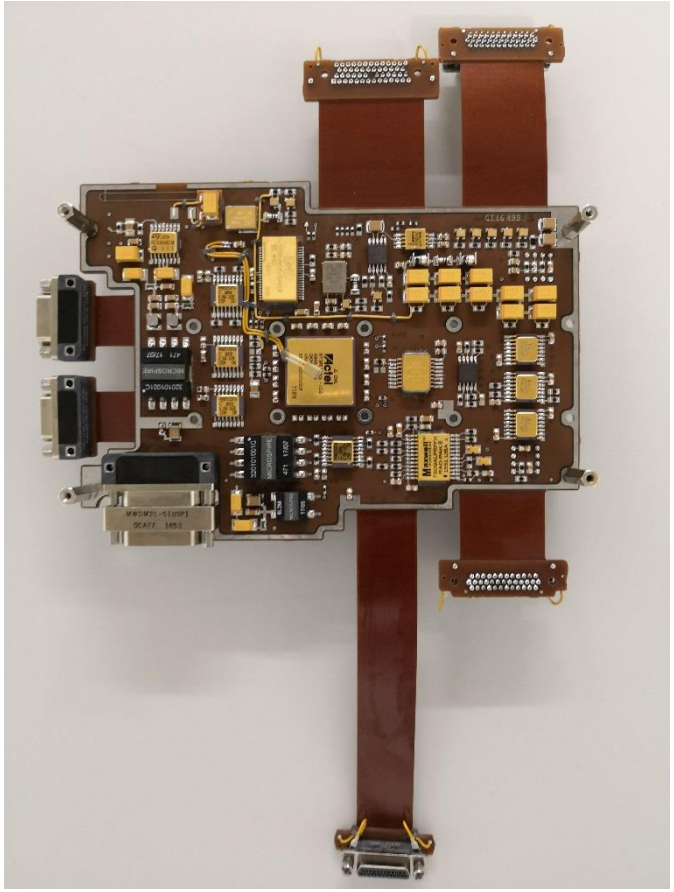


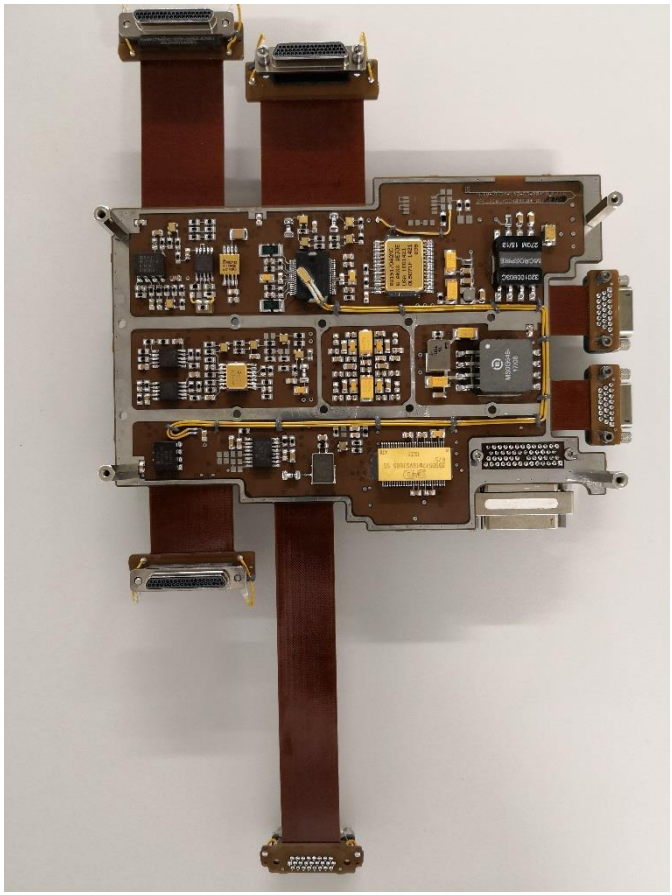


Jet Propulsion Laboratory
California Institute of Technology

MARS 2020 SUPER CAM

Carte de contrôle





Radiotélescope Géant SKA : Afrique du Sud

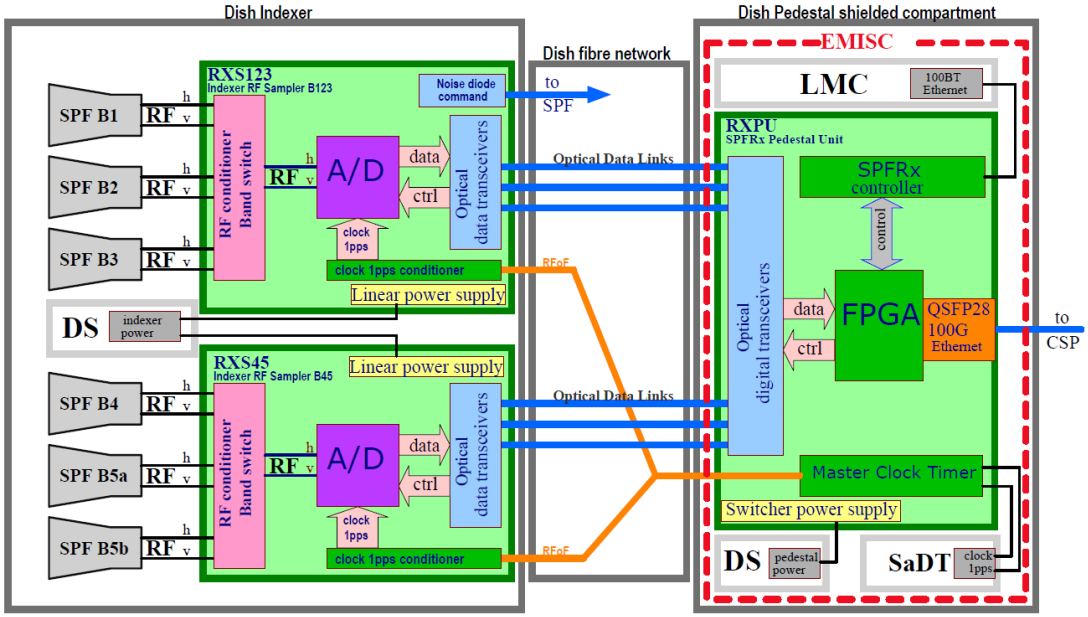
- Phase 1 (2020-2025) : Récepteur de la bande 5
  ⇒ 200 antennes à équiper
- Phase 2 (2025-2030) : 2000 antennes

		RF frequency range (GHz)	RF Bandwidth (GHz)	ADC sampling rate (GSps)	Minimal ADC sampling bit depth	Transport sampling rate (GSps)	Transport bit depth
RXS123	Band 1	0.35 – 1.05	0.70	4	8	4	8
	Band 2	0.95 – 1.76	0.81	4	8	4	8
	Band 3	1.65 – 3.05	1.40	3.2	6	3.2	8
RXS45	Band 4	2.80 – 5.18	2.38	16	4	6	8
	Band 5a	4.60 – 8.50	3.9	9	3	2x6	4
	Band 5b	8.30 – 15.40	7.1	16	3	2x6	4

Radiotélescope Géant SKA : Afrique du Sud

- Phase 1 (2020-2025) : Récepteur de la bande 5

⇒ 200 antennes à équiper



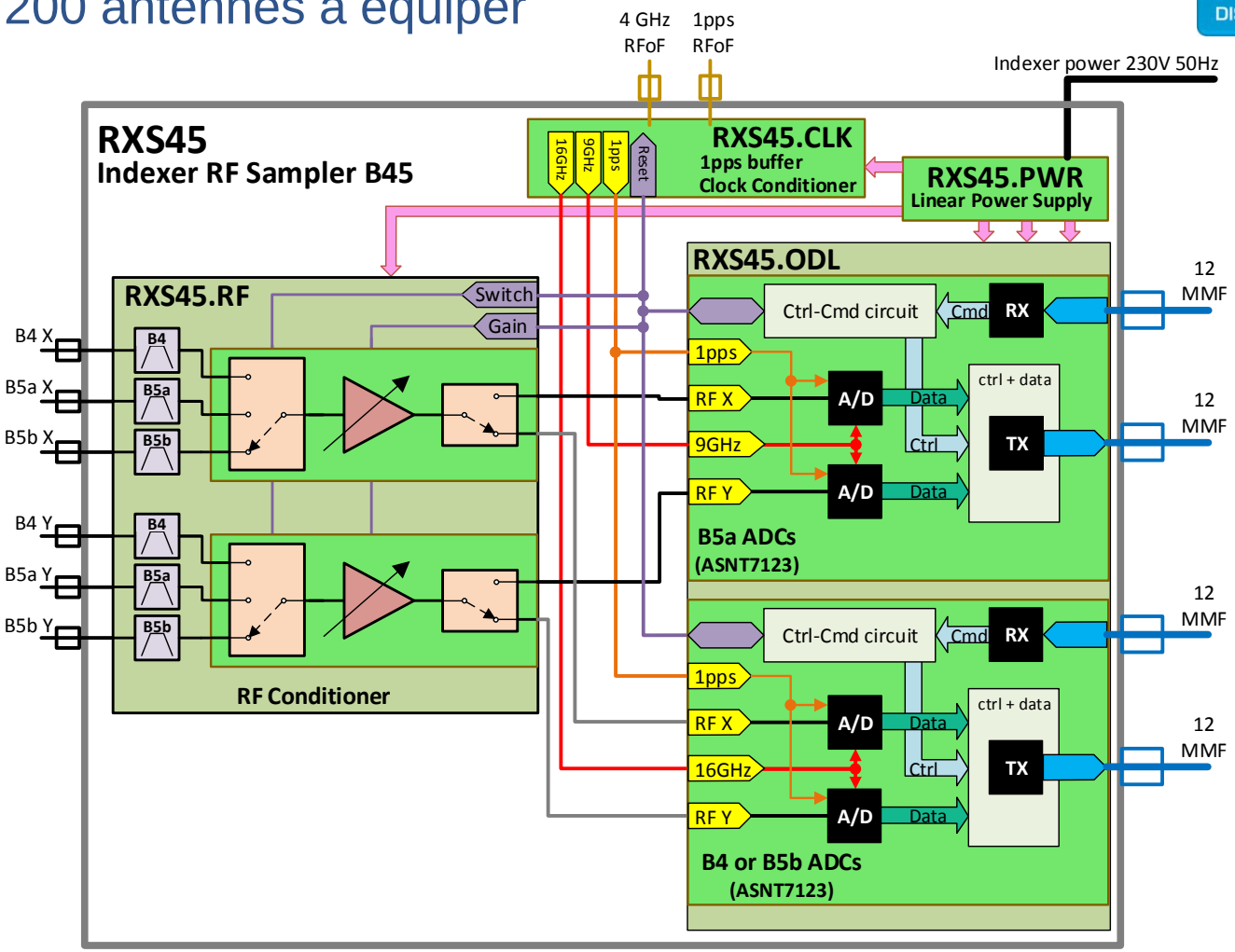
SPFRx Pedestal Unit

SPFRx Indexer Sampler

Radiotélescope Géant SKA : Afrique du Sud

- Phase 1 (2020-2025) : Récepteur de la bande 5

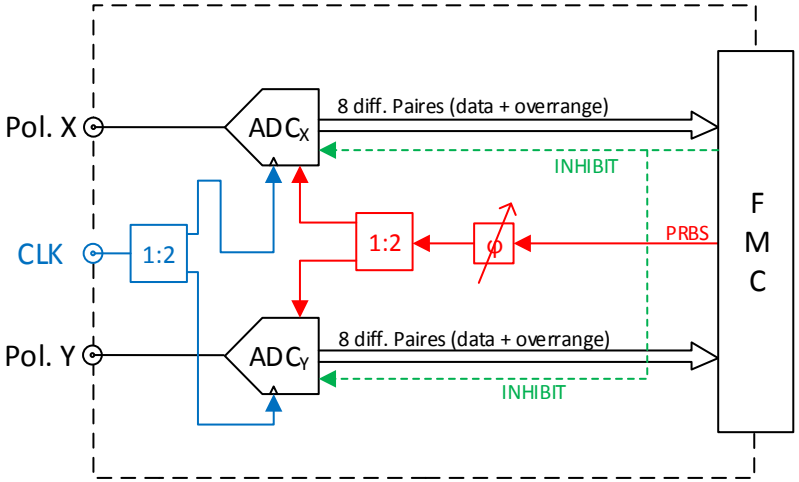
⇒ 200 antennes à équiper

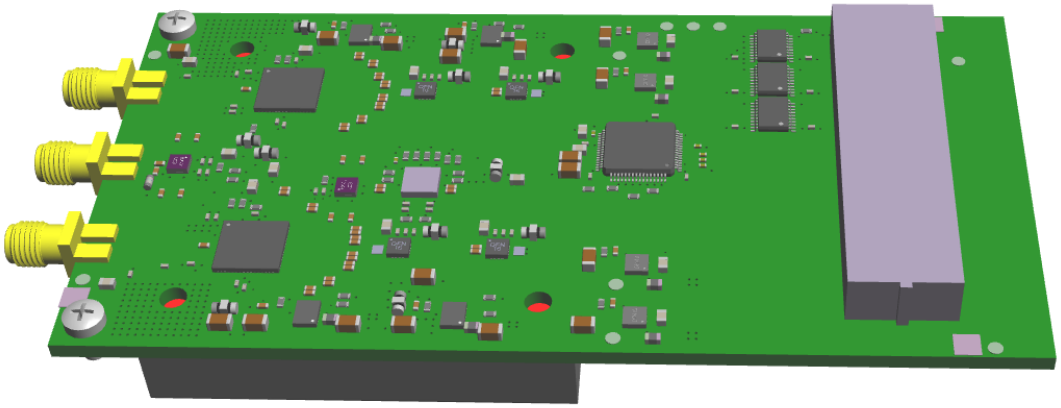


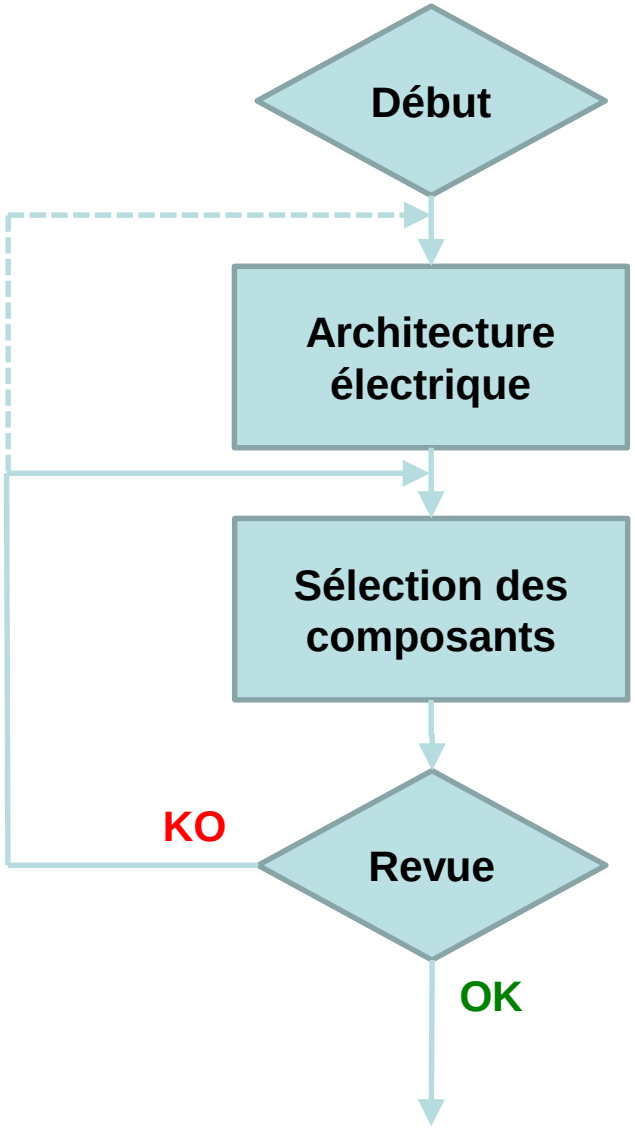
Radiotélescope Géant SKA : Afrique du Sud

- Phase 1 (2020-2025) : Récepteur de la bande 5

⇒ 200 antennes à équiper





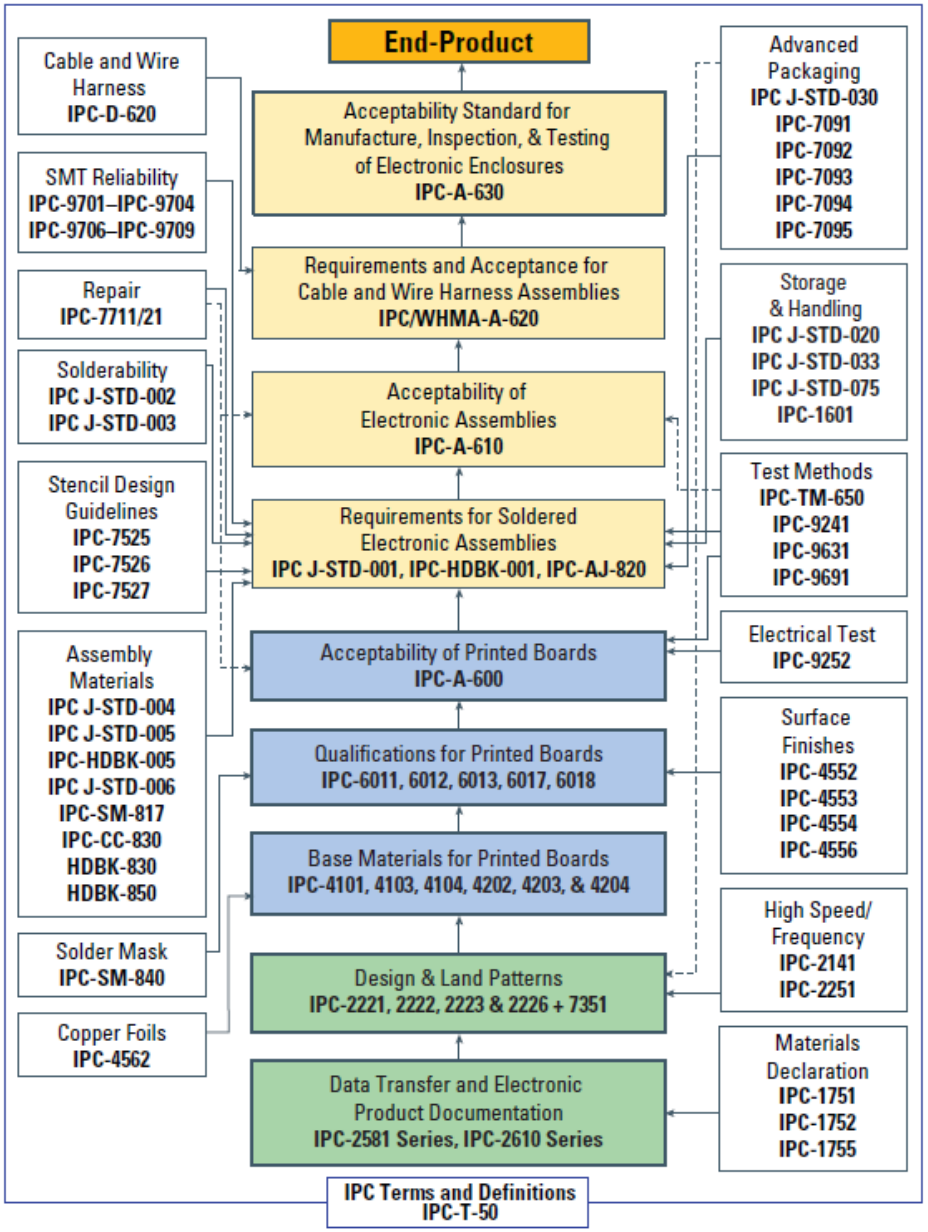


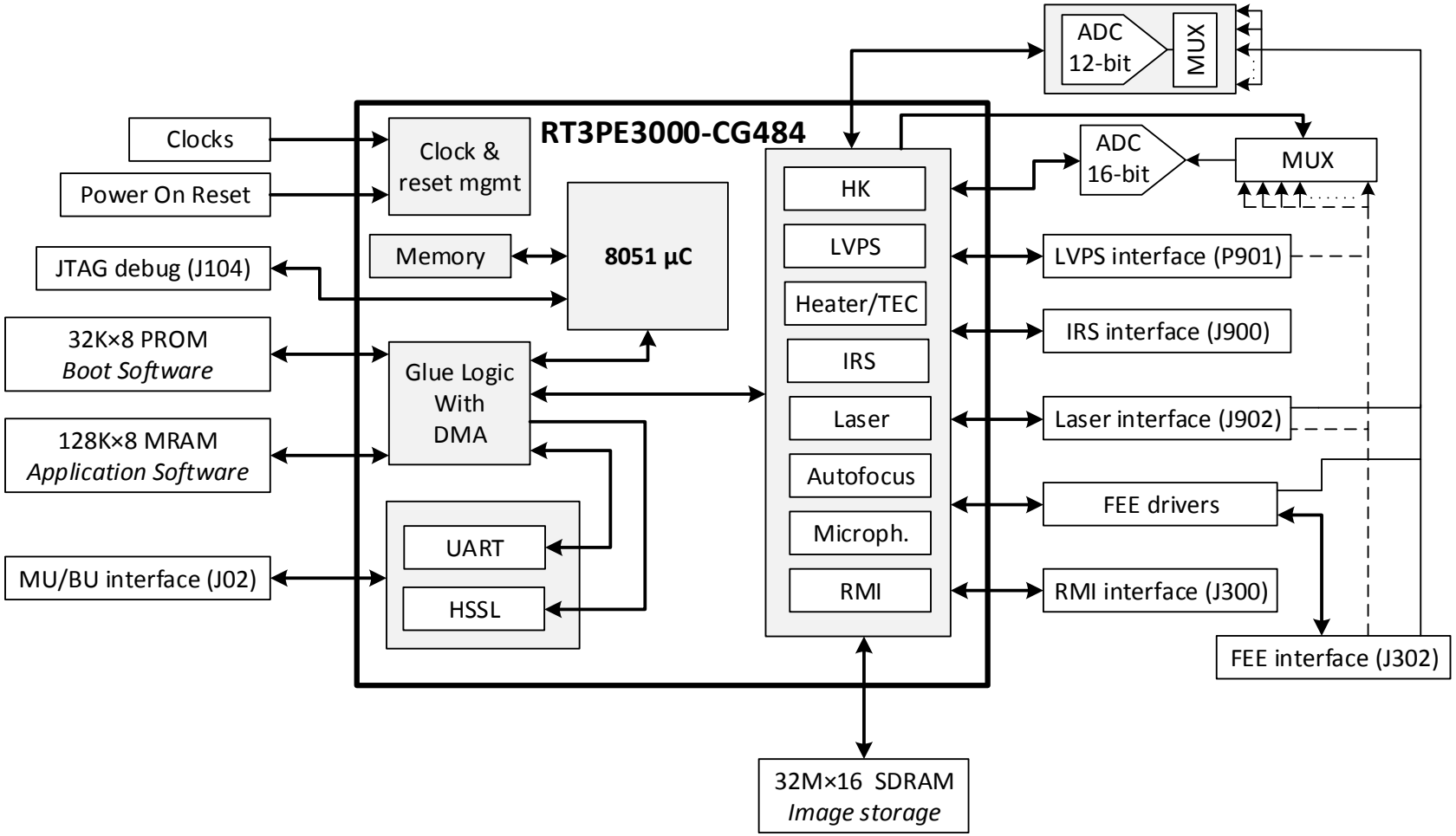
- L'application
- La finalité (prototype, production)
- Les normes (IPC, ESA SCC)
- L'environnement (contraintes mécaniques, températures)
- Coût et délais

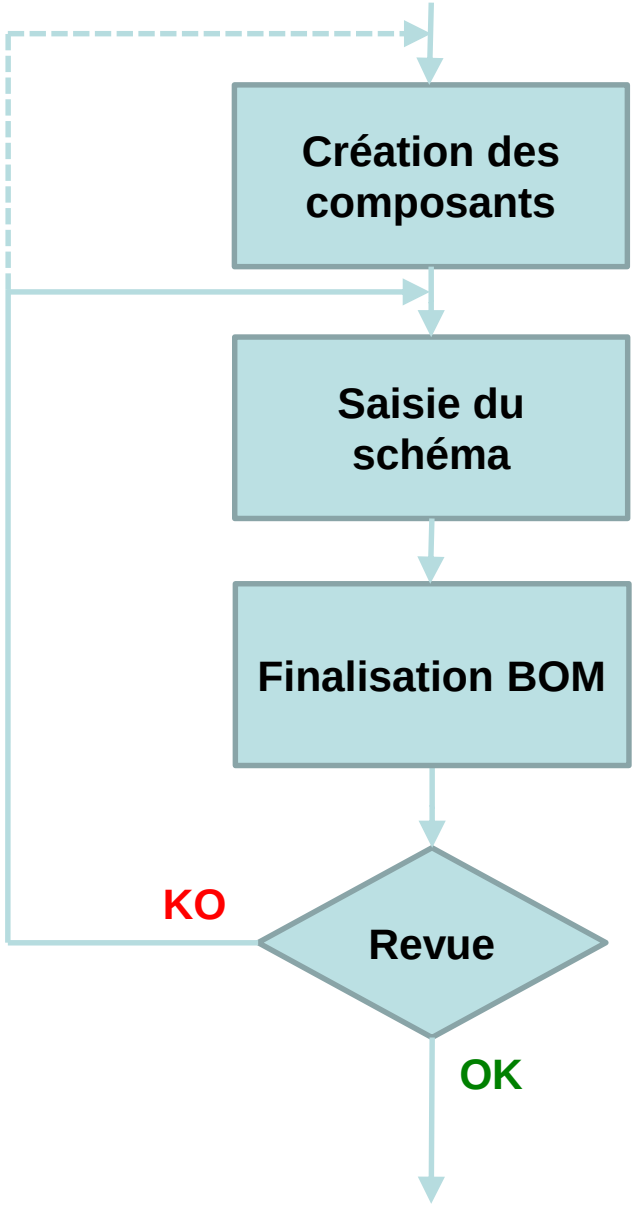
- Schéma bloc fonctionnel

- Mise en place de la BOM

- Analyse d'obsolescence
- Approvisionnement
- Analyse architecture


End-Product
Cable and Wire Harness IPC-D-620
SMT Reliability IPC-9701–IPC-9704 IPC-9706–IPC-9709
Repair IPC-7711/21
Solderability IPC J-STD-002 IPC J-STD-003
Stencil Design Guidelines IPC-7525 IPC-7526 IPC-7527
Assembly Materials IPC J-STD-004 IPC J-STD-005 IPC-HDBK-005 IPC J-STD-006 IPC-SM-817 IPC-CC-830 HDBK-830 HDBK-850
Solder Mask IPC-SM-840
Copper Foils IPC-4562
Acceptability Standard for Manufacture, Inspection, & Testing of Electronic Enclosures IPC-A-630
Requirements and Acceptance for Cable and Wire Harness Assemblies IPC/WHMA-A-620
Acceptability of Electronic Assemblies IPC-A-610
Requirements for Soldered Electronic Assemblies IPC J-STD-001, IPC-HDBK-001, IPC-AJ-820
Acceptability of Printed Boards IPC-A-600
Qualifications for Printed Boards IPC-6011, 6012, 6013, 6017, 6018
Base Materials for Printed Boards IPC-4101, 4103, 4104, 4202, 4203, & 4204
Design & Land Patterns IPC-2221, 2222, 2223 & 2226 + 7351
Data Transfer and Electronic Product Documentation IPC-2581 Series, IPC-2610 Series
Advanced Packaging IPC J-STD-030 IPC-7091 IPC-7092 IPC-7093 IPC-7094 IPC-7095
Storage & Handling IPC J-STD-020 IPC J-STD-033 IPC J-STD-075 IPC-1601
Test Methods IPC-TM-650 IPC-9241 IPC-9631 IPC-9691
Electrical Test IPC-9252
Surface Finishes IPC-4552 IPC-4553 IPC-4554 IPC-4556
High Speed/ Frequency IPC-2141 IPC-2251
Materials Declaration IPC-1751 IPC-1752 IPC-1755
IPC Terms and Definitions IPC-T-50


ADC
12-bit
MUX
RT3PE3000-CG484
Clocks
Clock &
reset mgmt
Power On Reset
ADC
16-bit
MUX
HK
LVPS
Heater/TEC
IRS
Laser
Autofocus
Microph.
RMI
Memory
8051 µC
JTAG debug (J104)
LVPS interface (P901)
IRS interface (J900)
32K×8 PROM
Boot Software
Glue Logic
With
DMA
Laser interface (J902)
128K×8 MRAM
Application Software
FEE drivers
UART
HSSL
MU/BU interface (J02)
RMI interface (J300)
FEE interface (J302)
32M×16 SDRAM
Image storage

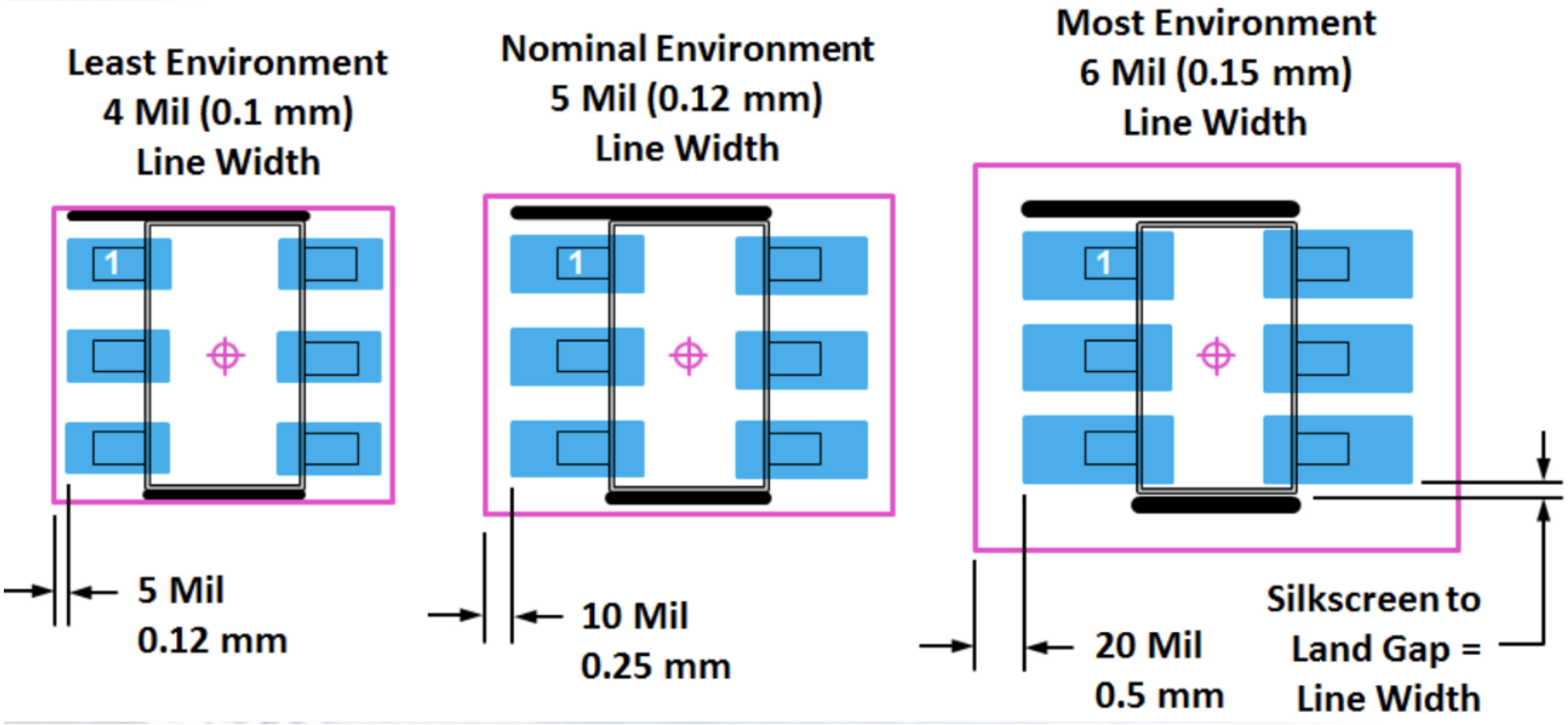


- « Datasheet » de chaque composant
- Symbole
- Empreinte (IPC-7351 ou fabricant)
- Vue 3D

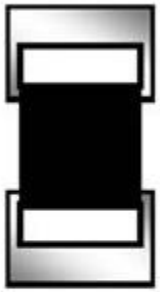
- Faire un schéma clair avec annotations
- Préparation au routage (renseigner les « nets »)
- Préparation au test (points de test, consommation)

- Vérification des symboles
- Vérification des empreintes
- Vérification de l'assignement des broches
- Analyse du schéma
- Analyse de la BOM (délais d'approvisionnement)

The preliminary recommendation for 3-Tier line widths and Silkscreen to Pad Gap are illustrated in the pictures below representing a SOT23-6 component package



Rectangular Two Terminal Devices

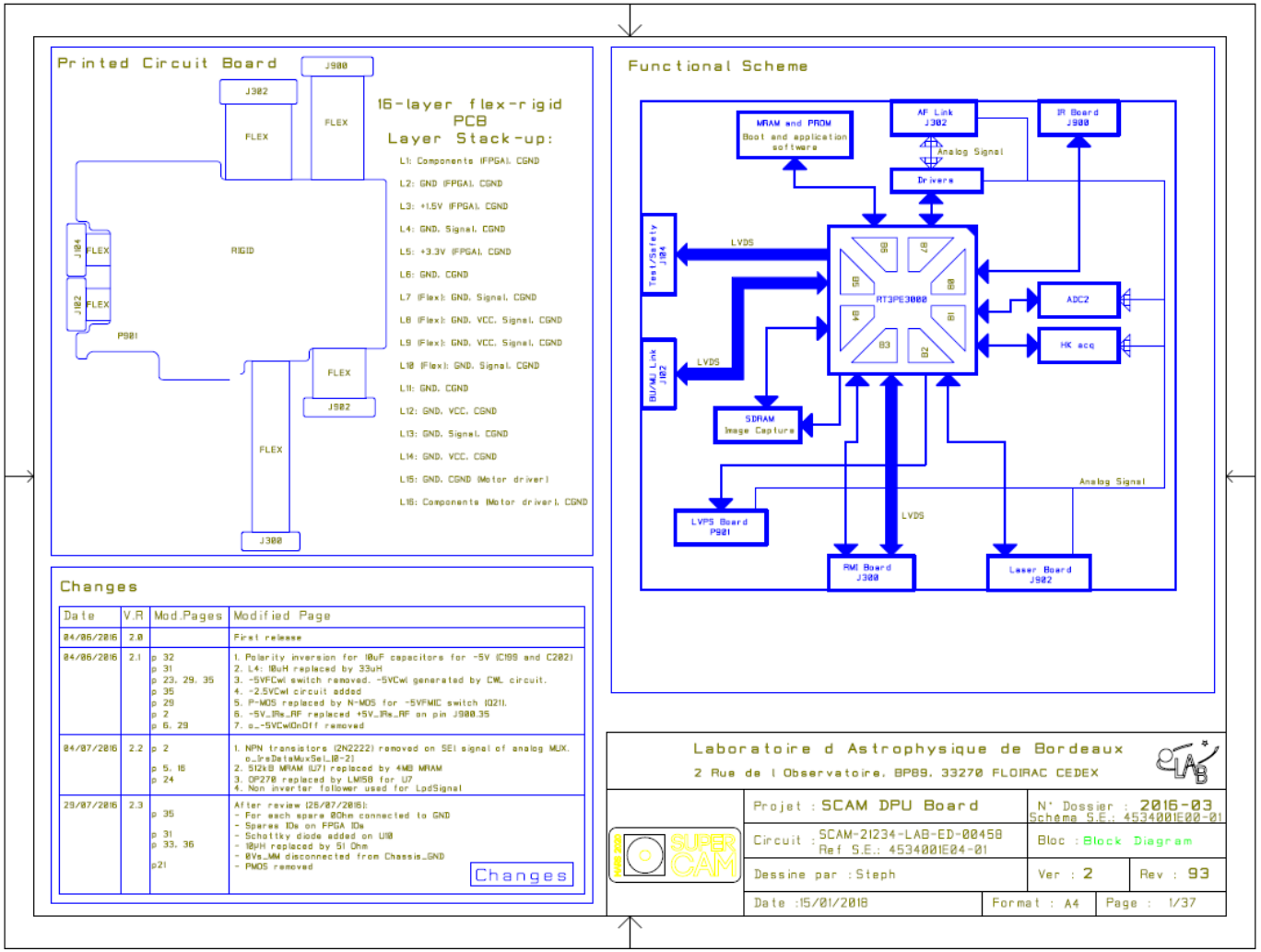


Level A
Very Robust
Solder Joint

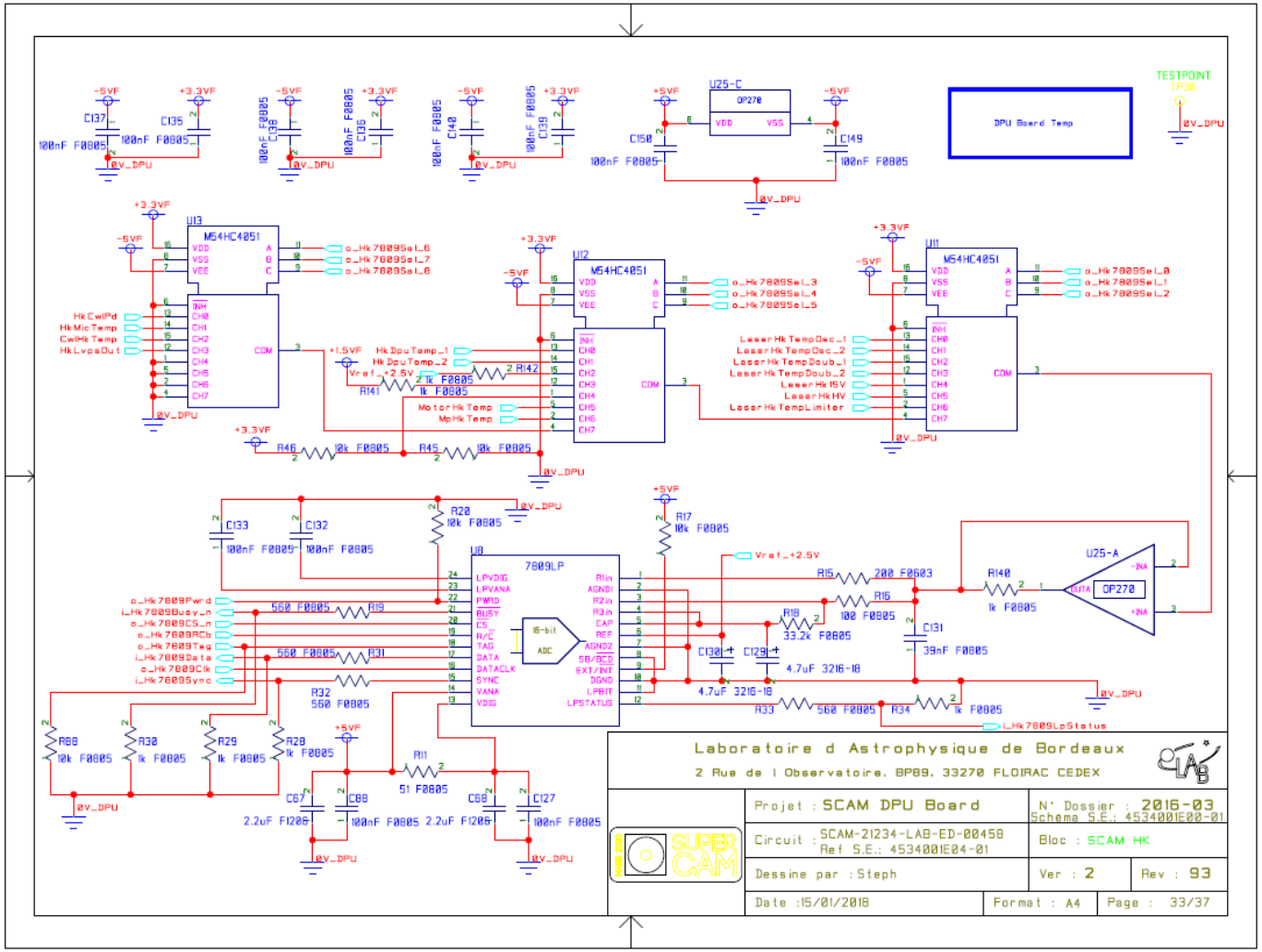
Level B
General Purpose
Solder Joint

Level C
Minimal Solder Joint
for
High Density Applications

- **Hiérarchie : page de garde avec schéma bloc**
- **Tableau de modifications (version)**

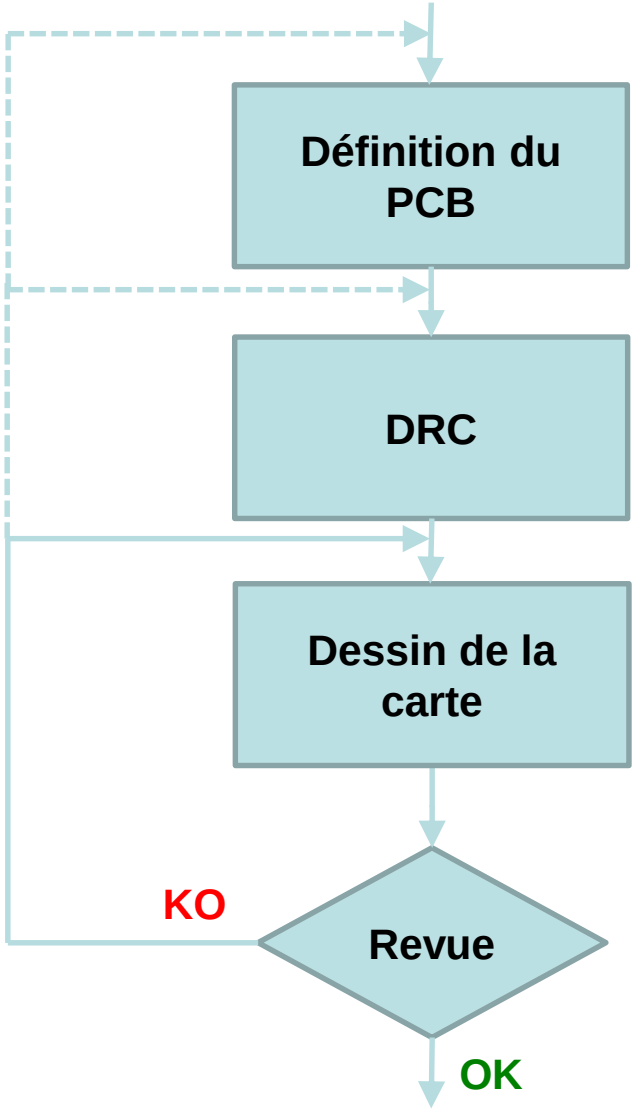


- **Symboles reliés par des fils de connexion (« nets »)**



- **Masse**
- **Alimentation**
- **Signal**
- **Horloge**
- **« Single-Ended » ⇒ impédance contrôler (50 Ohms)**
- **« Différentiels » ⇒ impédance contrôler (100 Ohms)**

Item	Quantité	Nom	Description	Boitier	Valeur	Tension	Tolérance	Fabricant	Référence fabricant	Distributeur	Réf.Distributeur
1	24	C122-124, C129, C135, C141, C142, C157, C172, C177, C178, C181, C188, C193, C194, C197, C200, C206, C210-212, C214, C220, C227	1µF, SM Ceramic Capacitor, X5R, 0805	0805	1µF	50V	± 10%	KEMET	C0805C105K5RACTU	Digikey	399-7409-6-ND
10	22	EMI5-9, EMI13-20, EMI25, EMI29-31, EMI34-38	SM EMI Filter, NFE31PT Series, 2200pF	NFE31PT	NFE31PT			Murata	NFE31PT222Z1E9L	Digikey	490-2547-1-ND
11	8	FB1-8	SM EMI Suppression Ferrite Bead	0805	220Ohm at 100MHz			Wurth	742792022	Digikey	732-1614-1-ND
12	1	J1	.05 Pitch Terminal Array Assembly		ASP-13448-01			Samtec	ASP-13448-01	Farnell	2433503
13	3	J4, J7, J8	SMA End Launch Connectors		142-0761-811			Amphenol	142-0761-811	Digikey	J798-ND
14	1	J5	Surface Mount Connector, 4 positions, Low profile		DF65-4P-1.7V			Hirose	DF65-4P-1.7V(21)	Mouser	798-DF65-4P-1.7V(21)
15	1	PCB	Printed Circuit Board, 10-layers, Megtron 6							Atlantec	
27	2	R41, R59	14k7, SM Resistor, 0603	0603	14k7		±1%	Vishay Dale	CRCW060314K7FKEA	Digikey	541-51.0KHCT-ND
28	4	R50, R53, R56, R64	51k, Surface Mount Resistor, 0603	0603	51k		±1%	Vishay Dale	CRCW060351K0FKEA		
30	4	R6, R8, R14-15	1k, SM Resistor, 0402	0402	1k		±1%	Vishay Dale	CRCW04021K00FKED	Digikey	541-1.00KLCT-ND
31	4	R73, R76, R105, R108	49.9, SM Resistor, 0402	0402	49,9		±1%	Vishay Dale	CRCW040249R9FKED	Digikey	541-49.9LCT-ND
32	2	R81, R82	200, SM Resistor, 0603	0603	200		±1%	Vishay Dale	CRCW0603200RFKEAHP	Digikey	541-200SCT-ND
33	1	SINK1	Heat Sink for Half Brick DC/DC Converter					AAVID Thermalloy	241214B91200G	Farnell	1436803
34	2	U1, U2	3-bit, 26GSps Analog-to-Digital Converter with Overrange, inhibit, and 1:2 DMUX	QFN68	HMCAD5831			ADI	HMCAD5831LP9BE	Fourni par le LAB	
35	2	U10, U11	8-bit Bidirectional Voltage-Level translator with Auto-Direction Sensing	TSSOP20	TXB0108			TI	TXB0108PWR	Mouser	595-TXB0108PWR
36	2	U12, U16	SMT GaAs HBT MMIC, Divide-by-8, DC-18GHz	LP3E	HMC494			ADI	HMC494LP3E	Digikey	1127-3561-2-ND
37	2	U14, U17	SMT GaAs HBT MMIC, Divide-by-4, DC-18GHz	LP3E	HMC493			ADI	HMC494LP3E	Digikey	1127-3515-1-ND
38	4	U15, U18, U22, U23	20V, 500mA, Ultralow Noise Linear Regulator	DFN10	LT3045			Linear Technology	LT3045IDD#PBF	Digikey	LT3045IDD#PBF-ND
39	1	U19	Octal Buffer/Line Drivers, 3-State, Non-Inverting	SSOP20	CD74AC541			TI	CD74AC541SM96	Digikey	296-31547-1-ND
40	4	U29, U31, U32, U34	16-bit SPI nanoDAC, Vlogic from 1.62V to 5.5V	LFCSP-8	AD5683R-1			ADI	AD5683RACPZ-1RL7	Digikey	AD5683RBCPZ-1RL7CT-ND
41	2	U30, U33	OVP and EMI Protected, Precision, Low Noise and Bias Current Op Amps	SOIC8	ADA4177			ADI	ADA4177-2ARZ	Digikey	ADA4177-2ARZ-ND
42	4	U5, U7, U20, U21	-36V, 1.5A Negative Linear Regulator with Programmable Current Limit	DFN14	LT3091			Linear Technology	LT3091IDE#PBF	Digikey	LT3091IDE#PBF-ND
43	1	U6	28 Gbps, 5-bit Digital Time Delay With Programmable Output Voltage	LC5	HMC856			ADI	HMC856LC5	Farnell	2465259
44	2	U8, U26	28 Gbps, 1:2 Fanout Buffer With Programmable Output Voltage	LC3	HMC850			ADI	HMC850LC3	Mouser	584-HMC850LC3
45	1	U9	Data Acquisition systems 6 Channel 16-bit	LQFP64	AD7606			ADI	AD7606BSTZ	Digikey	AD7606BSTZ-ND



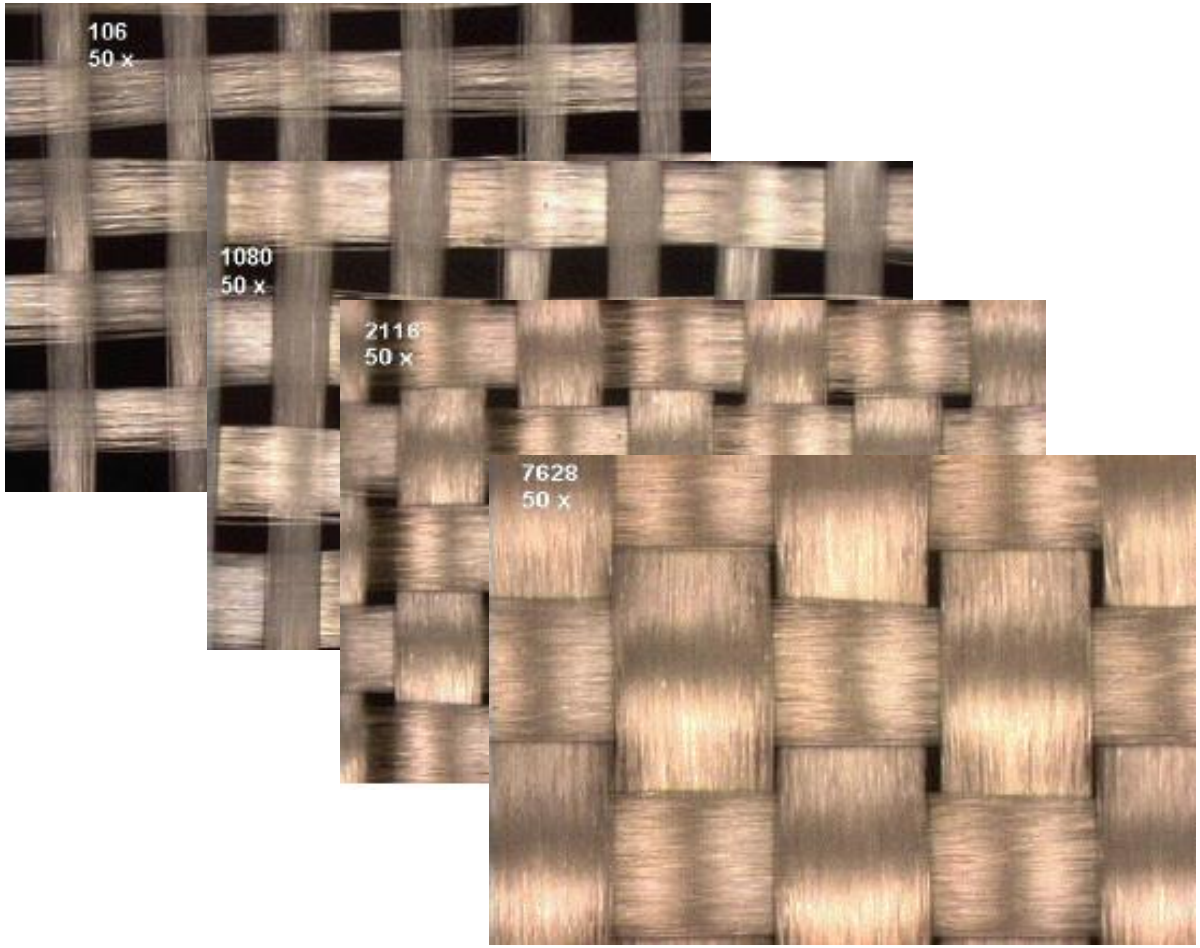
- Empilage de couches
- Lignes à impédance contrôlée
- Minimisation des effets de stubs
- Plan d'alimentation
- Thermique
- Mise en flan et panneau

- « Classe de routage » ⇒ DRC
- Contraindre le routage dans certaines zones ⇒ « Rules by area »

- Contraintes mécaniques et thermiques
- Placement des composants
- Carte d'évaluation de chaque composant
- Lignes à impédance contrôlée (skew)

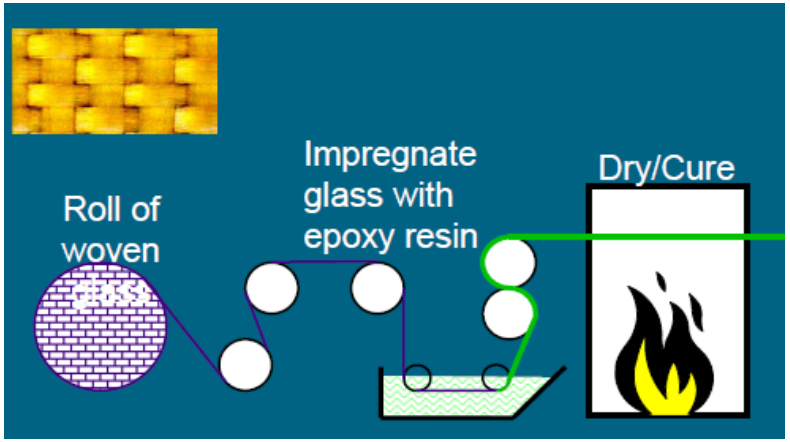
- Intégrité du signal
- Aucune violation de DRC
- Vérification des empreintes et assignement des broches
- Intégration dans mécanique (vue 3D)

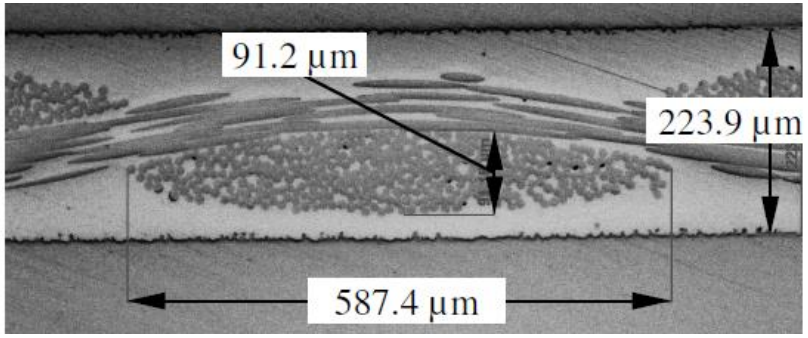
- **Préimprégné : un tissu de verre imprégné de résine**
- **Stratifié: un ou plusieurs préimprégnés entre deux feuillards de cuivre**

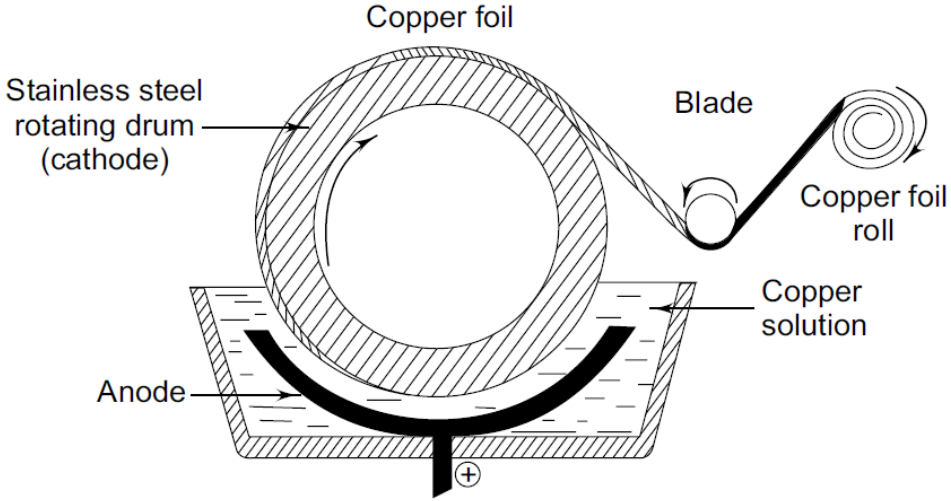


Glass Style	Resin Content (%)
106	73 ± 5
1080	62 ± 3
2113	58 ± 3
2116	50 ± 3
1506	44 ± 3
7628*	43 ± 3
7628*	47 ± 3
7628**	49 ± 3

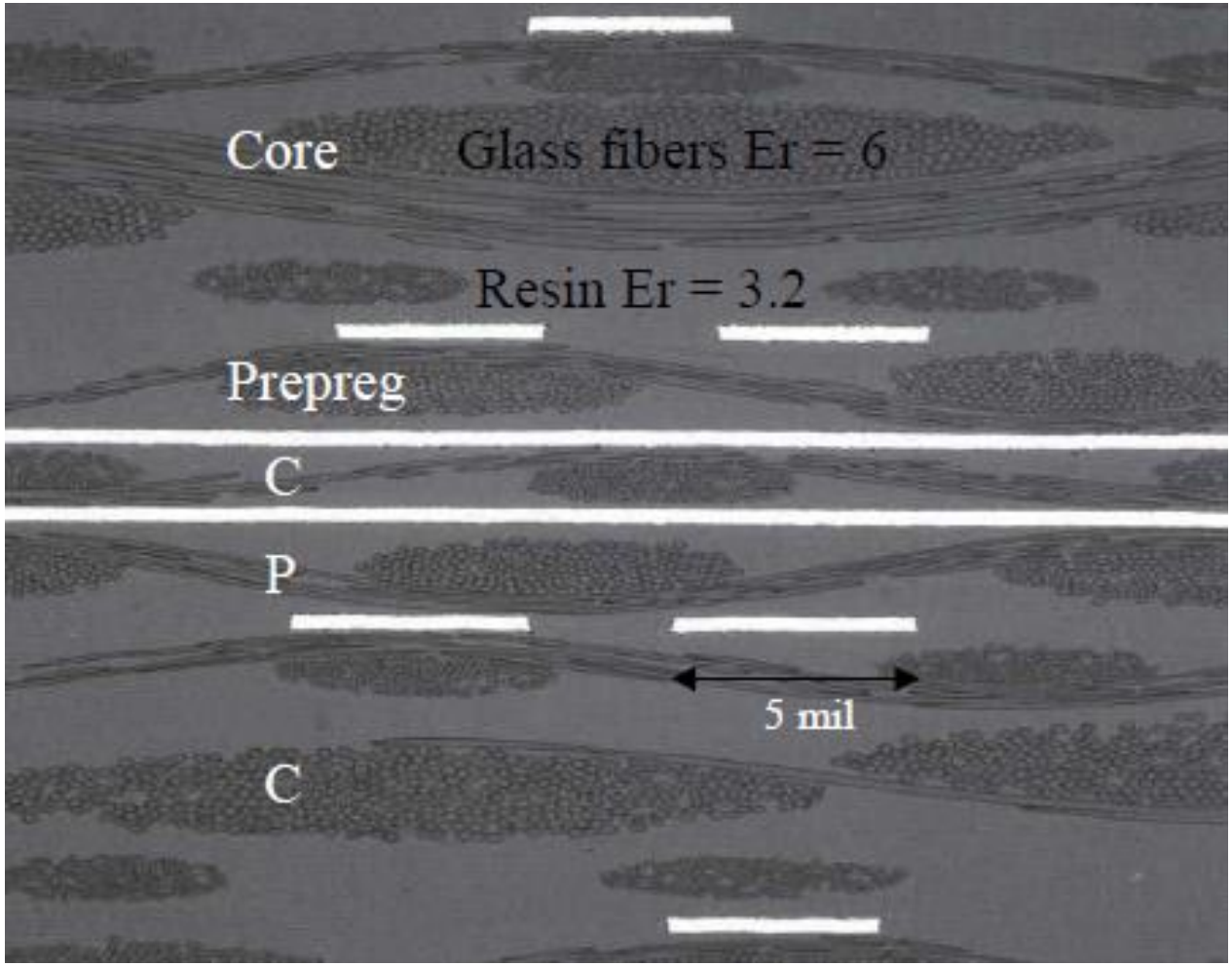
- **Préimprégné : un tissu de verre imprégné de résine**
- **Stratifié: un ou plusieurs préimprégnés entre deux feuillards de cuivre**

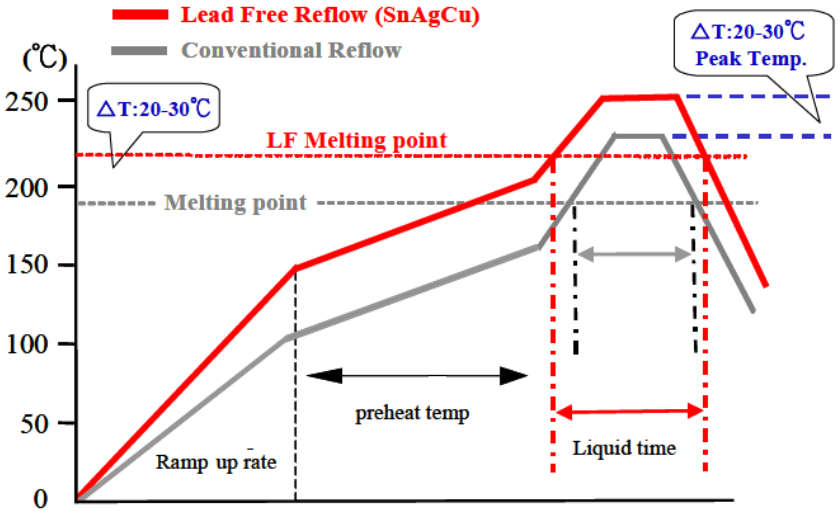


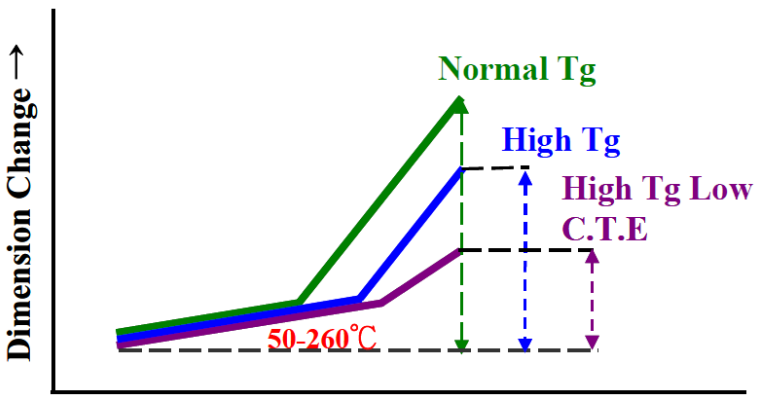




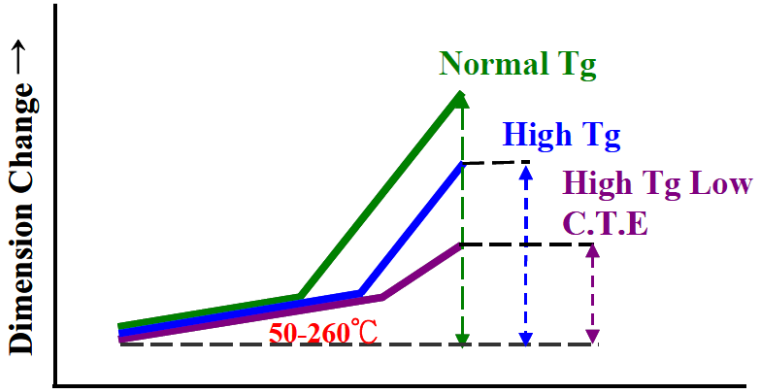
- **Préimprégné : un tissu de verre imprégné de résine**
- **Stratifié : un ou plusieurs préimprégnés entre deux feuillards de cuivre**



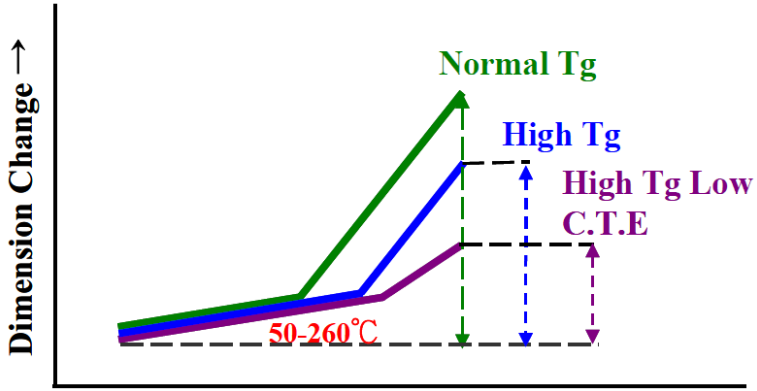


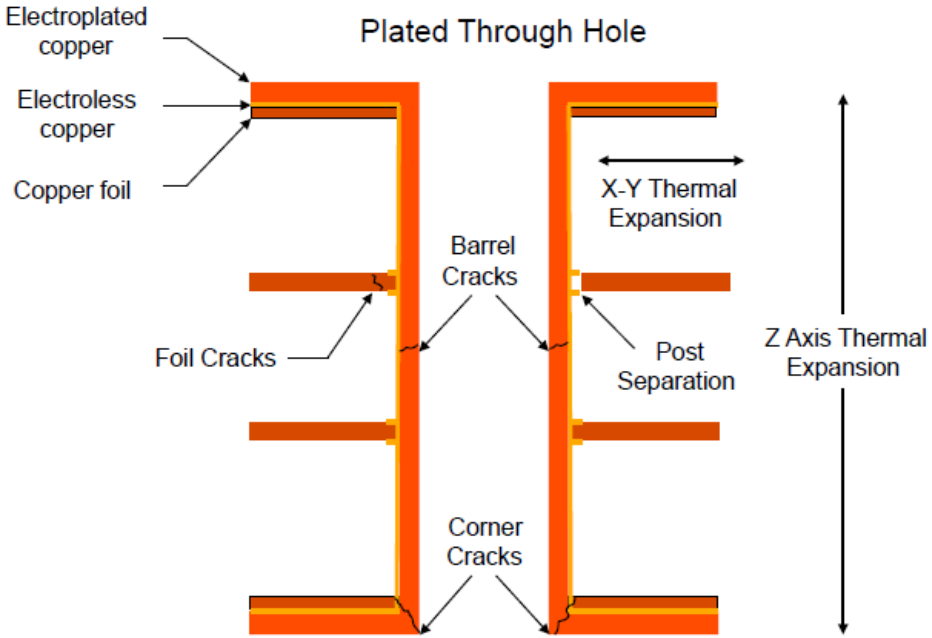


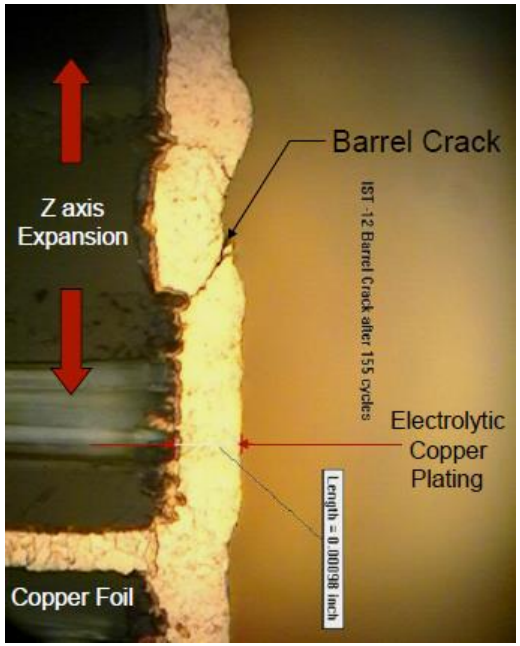
Type de stratifié	Tg	T260	T288
FR4 (PCLFR240 de Polyclad)	140°C		>10s
FR4 High Tg (IS410 d'Isola)	180°C	60mn	>20mn
BT (G200 d'Isola)	180°C		>10s
Cyanate Ester (N8000 de Nelco)	240°C	>60mn	>30mn
Polyimide (35N d'Arlon)	>250°C	>60mn	>60mn

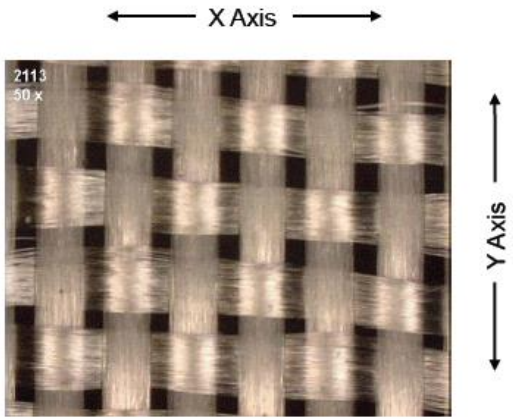


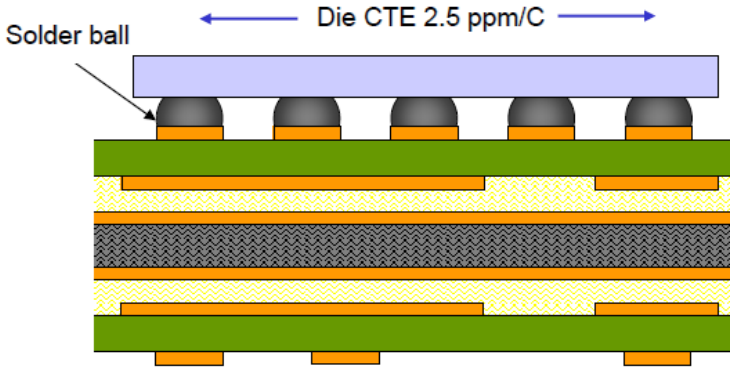
Type de stratifié	Tg	CTEz (<Tg)	CTEz (>Tg)
FR4 (PCLFR240 de Polyclad)	140°C	60 ppm/°C	250 ppm/°C
FR4 High Tg (IS410 d'Isola)	180°C	65 ppm/°C	250 ppm/°C
BT (G200 d'Isola)	180°C	55 ppm/°C	275 ppm/°C
Cyanate Ester (N8000 de Nelco)	240°C	70 ppm/°C	375 ppm/°C
Polyimide (35N d'Arlon)	>250°C	51 ppm/°C	158 ppm/°C


Dimension Change →
Normal Tg
High Tg
High Tg Low
C.T.E
50-260℃

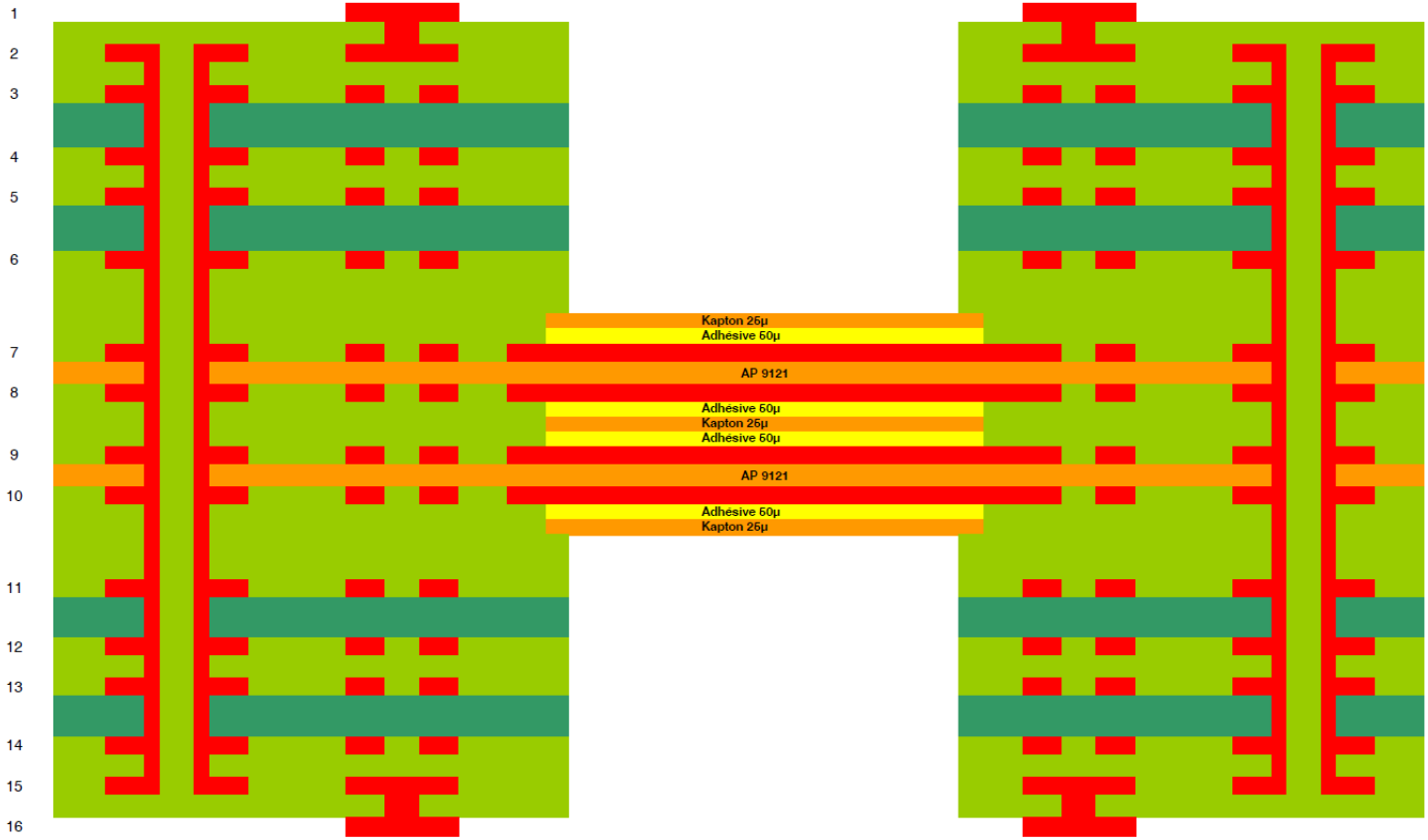

Plated Through Hole
Electroplated copper
Electroless copper
Copper foil
X-Y Thermal Expansion
Barrel Cracks
Foil Cracks
Post Separation
Z Axis Thermal Expansion
Corner Cracks


Z axis Expansion
Copper Foil
Barrel Crack
IST -12 Barrel Crack after 155 cycles
Electrolytic Copper Plating
Length = 0.00098 inch





Type de stratifié	Tg	CTExy (<Tg)	CTExy (>Tg)
Silicium	N/A	2,8 ppm/°C	
Cuivre	N/A	17-18 ppm/°C	
FR4 (PCLFR240 de Polyclad)	140°C	15 ppm/°C	17 ppm/°C
FR4 High Tg (IS410 d'Isola)	180°C	11 ppm/°C	13 ppm/°C
BT (G200 d'Isola)	180°C	14 ppm/°C	15 ppm/°C
Cyanate Ester (N8000 de Nelco)	240°C	11-13 ppm/°C	
Polyimide (35N d'Arlon)	>250°C	16 ppm/°C	



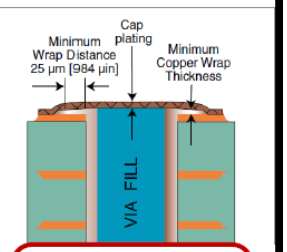
1	53	Cuivre	18 + 35
	80	Pré-Preg Arlon 35N	
2	43	Cuivre	18 + 25
	120	Pré-Preg Arlon 35N	
3	35	Cuivre	
	125	Matériau Arlon 35N	
4	35	Cuivre	
	120	Pré-Preg Arlon 35N	
5	35	Cuivre	
	125	Matériau Arlon 35N	
6	35	Cuivre	
	250	Pré-Preg Arlon 37N	
7	35	Cuivre	
	50	Kapton	
8	35	Cuivre	
	120	Pré-Preg Arlon 37N	
9	35	Cuivre	
	50	Kapton	
10	35	Cuivre	
	250	Pré-Preg Arlon 37N	
11	35	Cuivre	
	125	Matériau Arlon 35N	
12	35	Cuivre	
	120	Pré-Preg Arlon 35N	
13	35	Cuivre	
	125	Matériau Arlon 35N	
14	35	Cuivre	
	120	Pré-Preg Arlon 35N	
15	43		18 + 25
	80	Pré-Preg Arlon 35N	
16	53	Cuivre	18 + 35

1490	Ep du core
2366	Ep sur laminé
2472	Ep Totale

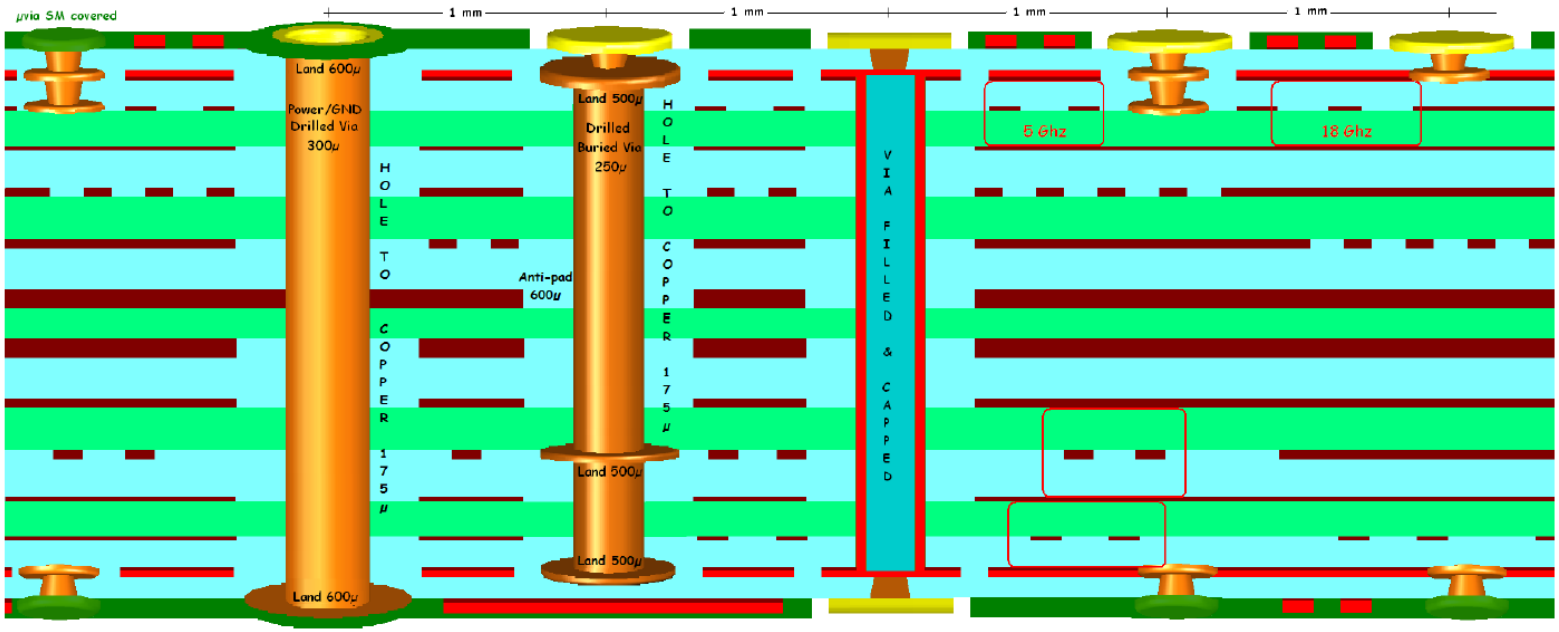
W@C5 : PCB HDI Interconnections description

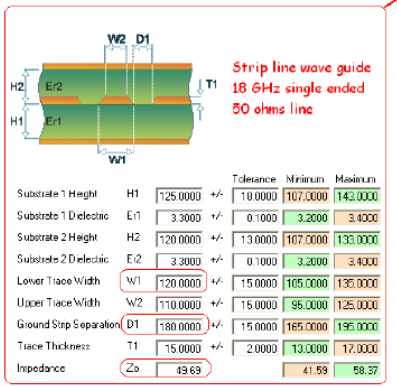
IPC
CID+
Certified Interconnect Designer
Advanced

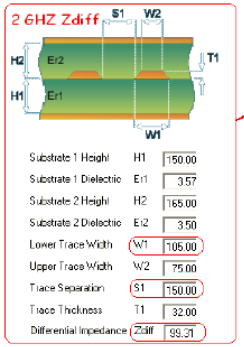
IPC 2226 type 3	Level A for laser drill at capture/target lands, Level C for the laser µvia land sizes
Via considerations	Skip PTH via as the non functional lands are dynamically removed by the CAD operator
Manufacture allowance	150µ AABUS (Hole to copper 175µ), format 18" x 24", pin-lam process is recommended
Annular ring IPC2	Level C for PTH L1/L14, AABUS (500µ mini) for the buried via L2/L13
PTH Via ratio	L1/L14 :drill 7.2:1 ratio level B
Buried via ratio	L2/ L9 :drill 8:1 ratio level C
Buried Via protection	Type 7 as resin filled and capped is used for the POVF (Plating Over Via Fill) process
Via & µvia Resin filler	Type :HITACHI GEA 679F(R)/TAYO THP 100DX1VF(HV), Vaccum process is recommended
Blind laser µvia	150µ, L1/L2 & L14/L13, µvia ratio 0.58:1 level B, Copper filled VIP for SMD
Buried laser µvia	150µ L2/L3, µvia ratio 0.78:1 level B, Resin filled and capped µvias
Special operation	1 Non plated Cavity 3 x 3 mm made by laser or by mechanical depth routing +/- 35µ

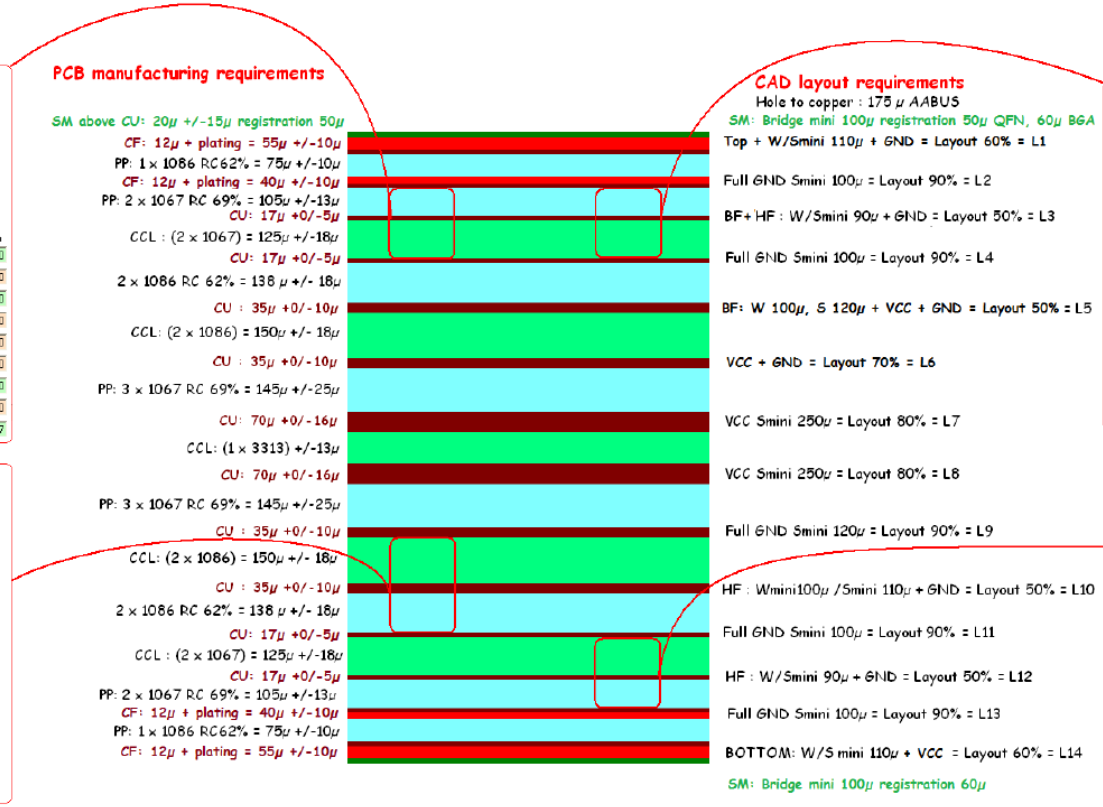


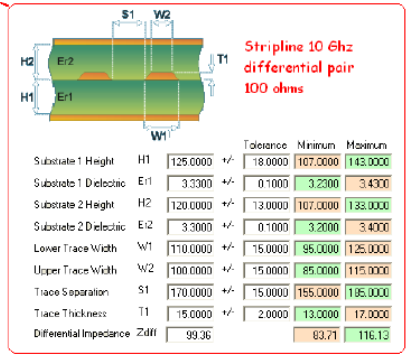
Class 3 is required as a minimum copper plating for the cap plating (POFV) L2/L9

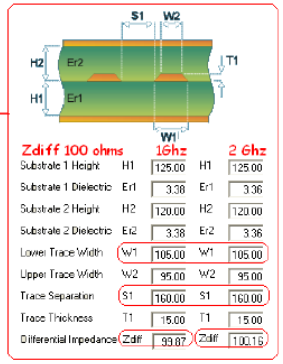


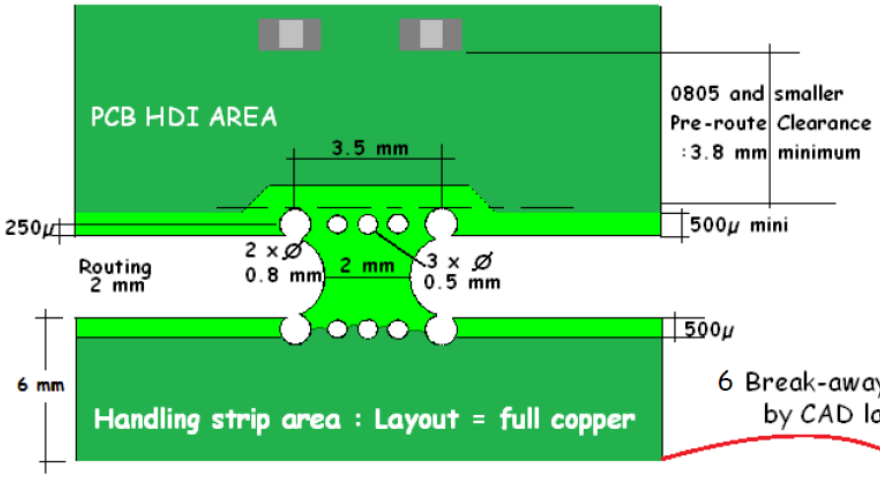

W2 D1
H2
Er2
T1
H1
Er1
W1
Strip line wave guide
18 GHz single ended
50 ohms line
Tolerance Minimum Maximum
Substrate 1 Height H1 125.0000 +/- 18.0000 107.0000 143.0000
Substrate 1 Dielectric Er1 3.3300 +/- 0.1000 3.2300 3.4300
Substrate 2 Height H2 120.0000 +/- 13.0000 107.0000 133.0000
Substrate 2 Dielectric Er2 3.3000 +/- 0.1000 3.2000 3.4000
Lower Trace Width W1 120.0000 +/- 15.0000 105.0000 135.0000
Upper Trace Width W2 110.0000 +/- 15.0000 95.0000 125.0000
Ground Strip Separation D1 180.0000 +/- 15.0000 165.0000 195.0000
Trace Thickness T1 15.0000 +/- 2.0000 13.0000 17.0000
Impedance Zo 49.69 41.59 58.37

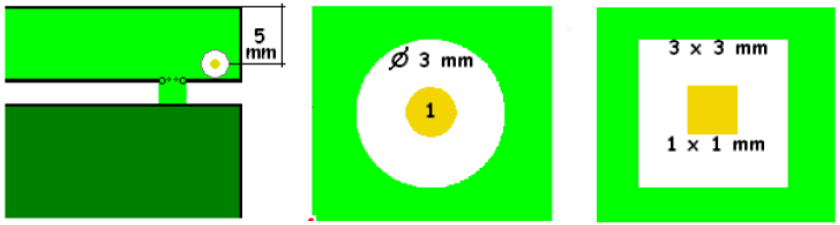

2 GHZ Zdiff
S1 W2
H2
Er2
T1
H1
Er1
W1
Substrate 1 Height H1 150.00
Substrate 1 Dielectric Er1 3.57
Substrate 2 Height H2 165.00
Substrate 2 Dielectric Er2 3.50
Lower Trace Width W1 105.00
Upper Trace Width W2 75.00
Trace Separation S1 150.00
Trace Thickness T1 32.00
Differential Impedance Zdiff 99.31


PCB manufacturing requirements
SM above CU: 20µ +/-15µ registration 50µ
CF: 12µ + plating = 55µ +/-10µ
PP: 1 x 1086 RC62% = 75µ +/-10µ
CF: 12µ + plating = 40µ +/-10µ
PP: 2 x 1067 RC 69% = 105µ +/-13µ
CU: 17µ +0/-5µ
CCL : (2 x 1067) = 125µ +/-18µ
CU: 17µ +0/-5µ
2 x 1086 RC 62% = 138 µ +/- 18µ
CU : 35µ +0/-10µ
CCL: (2 x 1086) = 150µ +/- 18µ
CU : 35µ +0/-10µ
PP: 3 x 1067 RC 69% = 145µ +/-25µ
CU: 70µ +0/-16µ
CCL: (1 x 3313) +/-13µ
CU: 70µ +0/-16µ
PP: 3 x 1067 RC 69% = 145µ +/-25µ
CU : 35µ +0/-10µ
CCL: (2 x 1086) = 150µ +/- 18µ
CU : 35µ +0/-10µ
2 x 1086 RC 62% = 138 µ +/- 18µ
CU: 17µ +0/-5µ
CCL : (2 x 1067) = 125µ +/-18µ
CU: 17µ +0/-5µ
PP: 2 x 1067 RC 69% = 105µ +/-13µ
CF: 12µ + plating = 40µ +/-10µ
PP: 1 x 1086 RC62% = 75µ +/-10µ
CF: 12µ + plating = 55µ +/-10µ
CAD layout requirements
Hole to copper : 175 µ AABUS
SM: Bridge mini 100µ registration 50µ QFN, 60µ BGA
Top + W/Smini 110µ + GND = Layout 60% = L1
Full GND Smini 100µ = Layout 90% = L2
BF+ HF : W/Smini 90µ + GND = Layout 50% = L3
Full GND Smini 100µ = Layout 90% = L4
BF: W 100µ, S 120µ + VCC + GND = Layout 50% = L5
VCC + GND = Layout 70% = L6
VCC Smini 250µ = Layout 80% = L7
VCC Smini 250µ = Layout 80% = L8
Full GND Smini 120µ = Layout 90% = L9
HF : Wmini100µ /Smini 110µ + GND = Layout 50% = L10
Full GND Smini 100µ = Layout 90% = L11
HF : W/Smini 90µ + GND = Layout 50% = L12
Full GND Smini 100µ = Layout 90% = L13
BOTTOM: W/S mini 110µ + VCC = Layout 60% = L14
SM: Bridge mini 100µ registration 60µ


S1 W2
H2
Er2
T1
H1
Er1
W1
Stripline 10 Ghz
differential pair
100 ohms
Tolerance Minimum Maximum
Substrate 1 Height H1 125.0000 +/- 18.0000 107.0000 143.0000
Substrate 1 Dielectric Er1 3.3300 +/- 0.1000 3.2300 3.4300
Substrate 2 Height H2 120.0000 +/- 13.0000 107.0000 133.0000
Substrate 2 Dielectric Er2 3.3000 +/- 0.1000 3.2000 3.4000
Lower Trace Width W1 110.0000 +/- 15.0000 95.0000 125.0000
Upper Trace Width W2 100.0000 +/- 15.0000 85.0000 115.0000
Trace Separation S1 170.0000 +/- 15.0000 155.0000 185.0000
Trace Thickness T1 15.0000 +/- 2.0000 13.0000 17.0000
Differential Impedance Zdiff 99.36 83.71 116.13

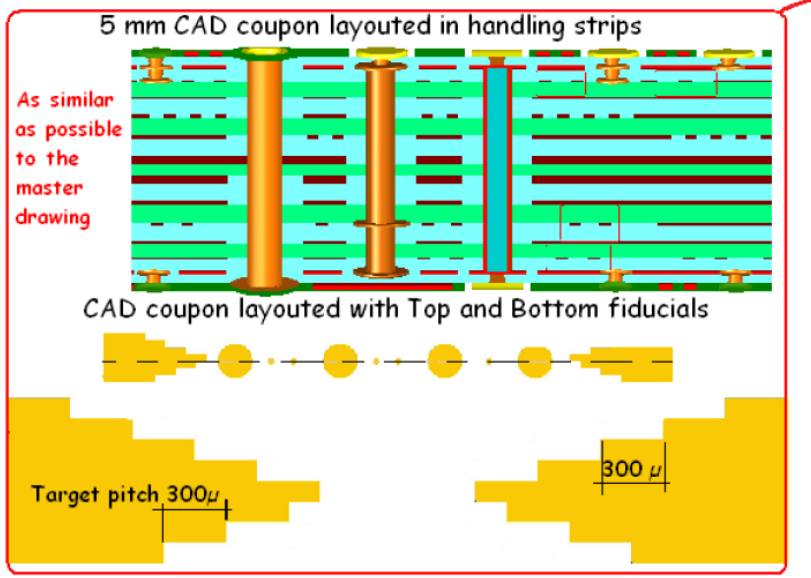

S1 W2
H2
Er2
T1
H1
Er1
W1
Zdiff 100 ohms
16hz
2 Ghz
Substrate 1 Height H1 125.00 H1 125.00
Substrate 1 Dielectric Er1 3.36 Er1 3.36
Substrate 2 Height H2 120.00 H2 120.00
Substrate 2 Dielectric Er2 3.36 Er2 3.36
Lower Trace Width W1 105.00 W1 105.00
Upper Trace Width W2 95.00 W2 95.00
Trace Separation S1 160.00 S1 160.00
Trace Thickness T1 15.00 T1 15.00
Differential Impedance Zdiff 99.87 Zdiff 100.16

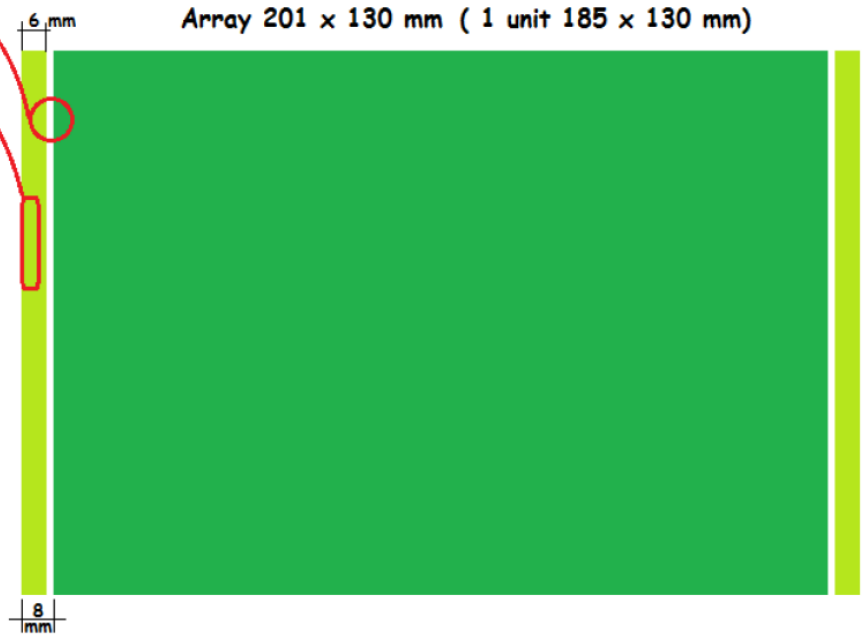




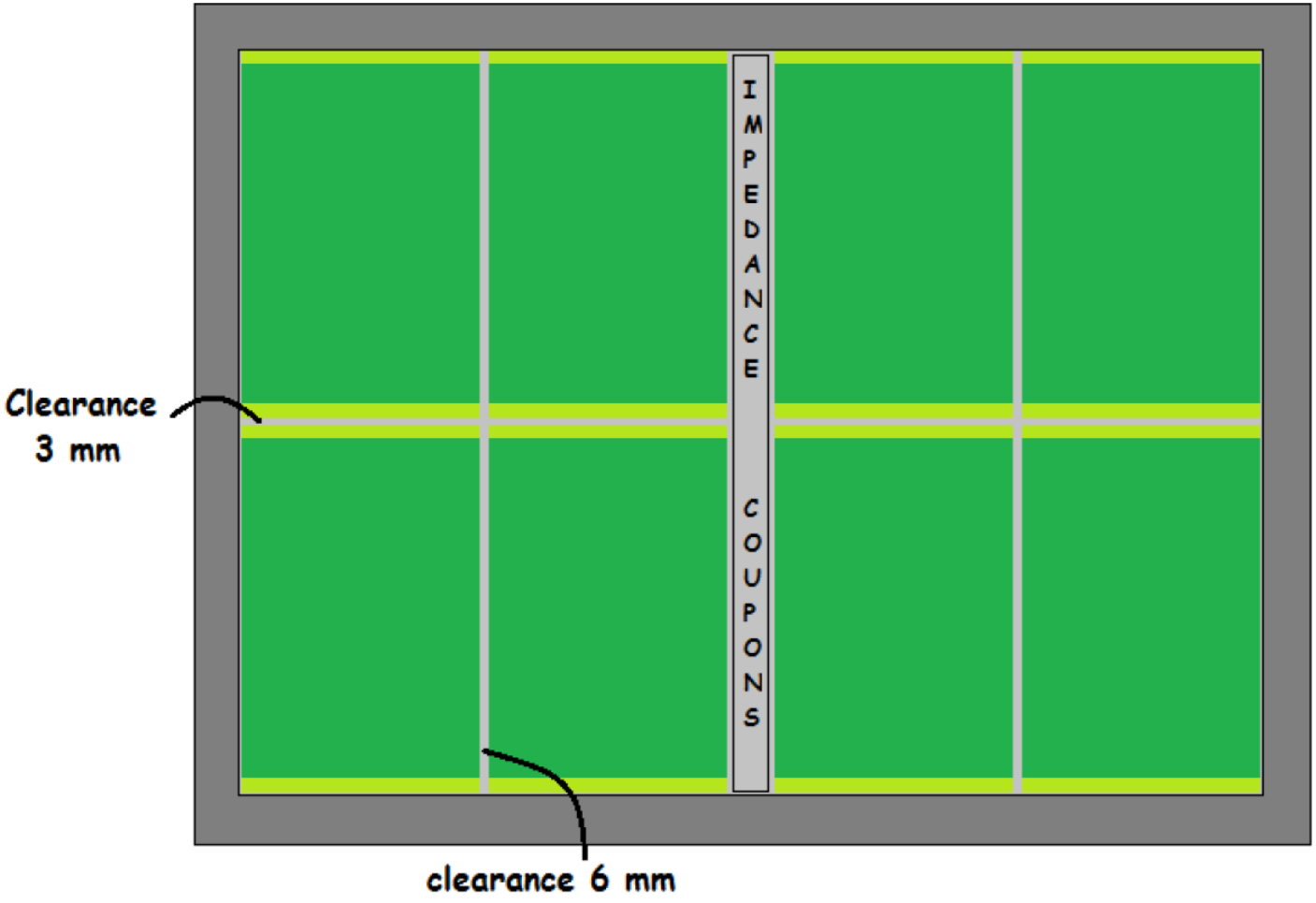
Fiducial type and location TBD

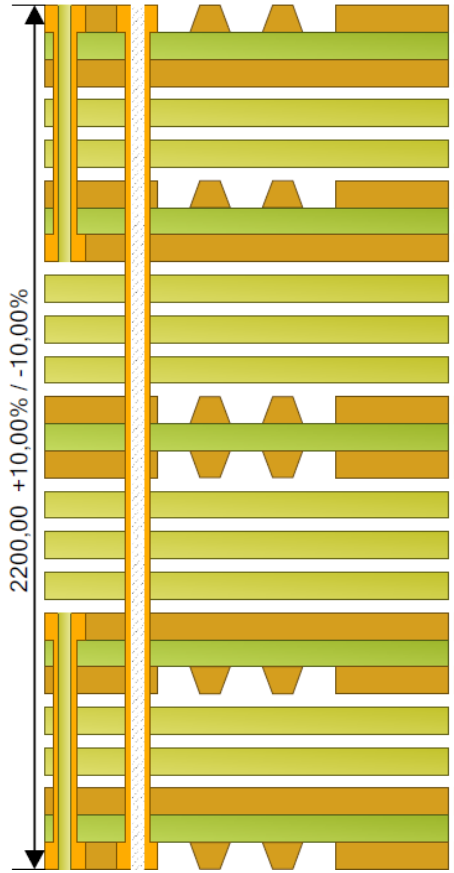
6 Break-away tabs
by CAD layout





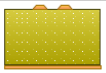
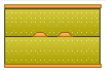
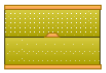
8 arrays 201 x 130 mm (1 unit 185 x 130 mm) on 18" x 24"
manufacturing format as 16" x 22" is the working area





Layer	Processed Thickness	Supplier Description	Copper Coverage	Impedance ID	Isolation Distance (Summed)
1	58,00		60,00	1, 2	
	250,00	F16_0.25_17_17_Megtron6_R-5775(K)			-
2	17,00		80,00		
	92,90	3313_Megtron6_R-5670(KF)_RC54%			185,80
	92,90	3313_Megtron6_R-5670(KF)_RC54%			-
3	17,00		60,00	3, 4	
	250,00	F16_0.25_17_17_Megtron6_R-5775(K)			250,00
4	25,00		80,00		
	71,83	1078_Megtron6_R-5670(KC)_RC64%			215,50
	71,83	1078_Megtron6_R-5670(KC)_RC64%			-
	71,83	1078_Megtron6_R-5670(KC)_RC64%			-
5	35,00		70,00		
	100,00	F16_0.1_35_35_Megtron6_R-5775(K)			100,00
6	35,00		70,00		
	71,83	1078_Megtron6_R-5670(KC)_RC64%			215,50
	71,83	1078_Megtron6_R-5670(KC)_RC64%			-
	71,83	1078_Megtron6_R-5670(KC)_RC64%			-
7	25,00		80,00		
	250,00	F16_0.25_17_17_Megtron6_R-5775(K)			250,00
8	17,00		60,00	5	
	92,90	3313_Megtron6_R-5670(KF)_RC54%			185,80
	92,90	3313_Megtron6_R-5670(KF)_RC54%			-
9	17,00		80,00		
	250,00	F16_0.25_17_17_Megtron6_R-5775(K)			250,00
10	58,00		60,00		

Q:\5000 NPI\Enregistrements\Empilages\Empilage_Excel & Speedstack\CNRS_UMR5804_SKAtelescope_MC10imp_27-03-2018.stk Units: Microns

Structure Image	Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Lower Ground Strip Width (G1)	Calculated Impedance	Target Impedance
	1	Surface Coplanar Waveguide With Lower Ground 1B	1	2	0	460,00	0,00	250,00	0,00	51,01	50,00
	2	Edge Coupled Surface Microstrip 1B	1	2	0	220,00	100,00	0,00	0,00	99,53	100,00
	3	Edge Coupled Offset Stripline 1B1A	3	2	4	120,00	100,00	0,00	0,00	100,32	100,00
	4	Offset Stripline 1B1A	3	2	4	210,00	0,00	0,00	0,00	51,13	50,00
	5	Edge Coupled Offset Stripline 1B1A	8	7	9	120,00	100,00	0,00	0,00	100,32	100,00

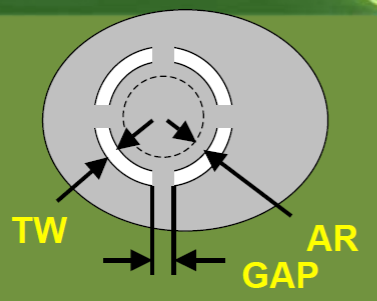
Notes

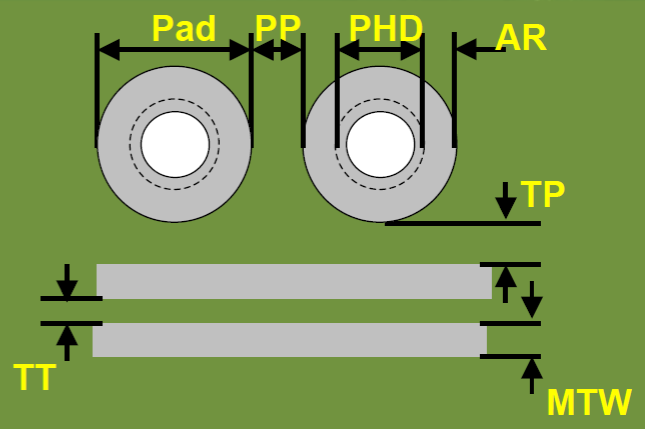
HDI DESIGN RULES: Classification

UNITS = µm	Design Rules Version 11/11/2010 ACB group	STANDARD						ADVANCED or ENGINEERING			
		Classification									
		3	4	5	6	7	8	9	10	11	12
Track & Gap	min Track to Track (TT) / Track to Pad (TP) / Pad to Pad (PP) Thermal Line Width (TW)	300	200	150	120	100	100	85	75	60	<
	min Track Width (MTW) / min Thermal Gap (GAP)	300	200	150	120	100	100	85	75	60	<
	Local fan out density (allowed on 10 % of the surface)	N A	N A	120	100	100	85	75	60	50	<
Ring for IPC Class 2	min Plated Layer Annular Ring (OAR) on Production Hole Diameter (PHD)	200	175	150	120	100	100	75	75	60	<
	min Inner Layer Annular Ring (IAR) / Thermal Annular Ring on PHD	225	200	175	145	125	125	100	100	85	<
Ring for IPC Class 3	min Plated Layer Annular Ring (OAR) on Production Hole Diameter (PHD)	250	225	200	170	150	150	125	125	110	<
	min Inner Layer Annular Ring (IAR) / Thermal Annular Ring on PHD	250	225	200	170	150	150	125	125	110	<
Aspect Ratio	max aspect ratio PTH: see table (Thickness / PHD)	see table	see table	see table	see table	see table	see table	see table	see table	see table	
Example for PCB with thickness 1.6mm											
Hole diameter	min PHD	500	450	400	350	300	250	250	200	150	<
IPC Class 2	min Plated Layer Pad Diameter	900	800	700	590	500	450	400	350	270	<
	min Inner Layer Pad Diameter	950	850	750	640	550	500	450	400	320	<
IPC Class 3	min Plated Layer Pad Diameter	1000	900	800	690	600	550	500	450	370	<
	min Inner Layer Pad Diameter	1000	900	800	690	600	550	500	450	370	<
µvia	min µvia top pad size				350	300	300	275	250	250	<
	min µvia landing pad size				350	300	300	275	220	220	<
	µvia diameter with dielectric 1 x 1080 prepreg				125	125	125	110	100	100	<
	µvia diameter with dielectric 2 x 106 prepreg (default)				150	150	150	130	N A	N A	<
	µvia diameter with dielectric 2 x 1080 prepreg				175	175	175	150	N A	N A	<
	max number of laserruns / side				1	2	3	4	4	4	>
Drill - Cu	distance PTH to Cu on inner layers (= TT/TP/PP + IAR class 2)	525	400	325	265	225	225	185	175	145	<
	distance PTH to PTH (= TT + 2 x IAR class 2 for standard)	750	600	500	410	350	350	285	275	230	<
	distance NPTH drill to Cu on inner layers (NPTH Routing always > 250 um)	IAR + 25	IAR + 25	IAR + 25	IAR + 25	IAR + 25	IAR + 25	IAR + 25	IAR + 25	IAR + 25	<
	distance NPTH to Cu on outer layers (NPTH Routing always > 200 um)	350	300	250	200	200	200	150	100	75	<
Cu Thickness	maximum total cu thickness that can be etched (no minimum)	105	70	60	50	35	35	20	15	15	<
	(Same trackwidth & bigger gap increases this value)	If Cu thickness is higher than the maximum for a class, class -> class +1									
Solder Mask	solder mask annular ring (MAR) & conductor overlap (MOC): typical	150	100	75	60	50	50	42,5	37,5	30	<
	solder mask annular ring (MAR) & conductor overlap (MOC): exceptional	100	70	50	43,5	37,5	30	25	25	25	<
	solder mask min segment (MSM) (If ACB creates SM, MSM >= 100)	200	150	125	100	100	100	87	87	75	<

▸ **PHD** = Production Hole Diameter = Final hole size + 100 for Component Holes if tolerance is symmetrical (+ 150 for HASL) ▸ **PHD** = Production Hole Diameter = Final hole size for Via Holes

HDI Design rules: Classification

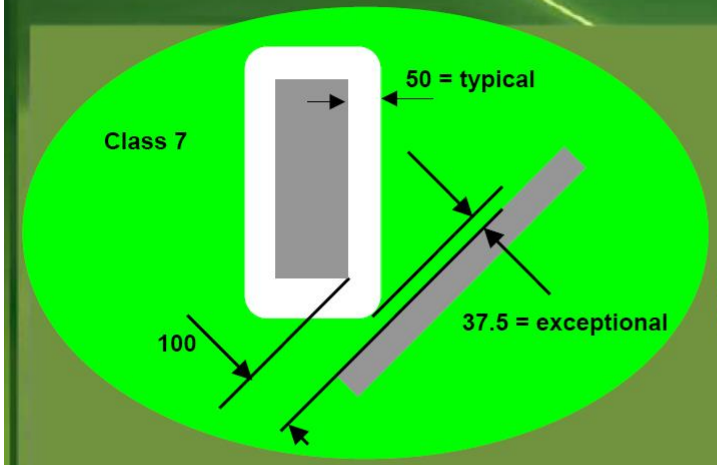




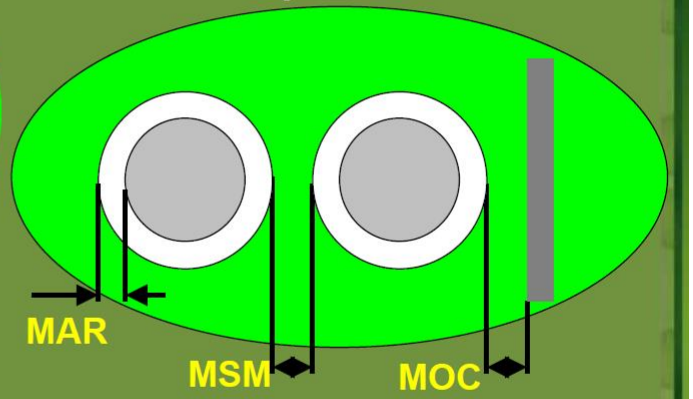
PHD =	Finished Hole size	+ 150 for PTH
		+ 100 for via holes
		+ 50 for NPTH

	Class					2008	2009	
	5	6	7	8	9	10	11	12
min TT / TP / PP / TW	150	125	100	87	75	60	50	<
min MTW / GAP	150	125	100	87	75	60	50	
min OAR	150	125	100	100	100	100	75	
min IAR / AR	175	150	150	125	125	100	75	
min PHD (for 1.6 mm)	400	350	300	250	250	200	150	
Aspect ratio - see table								

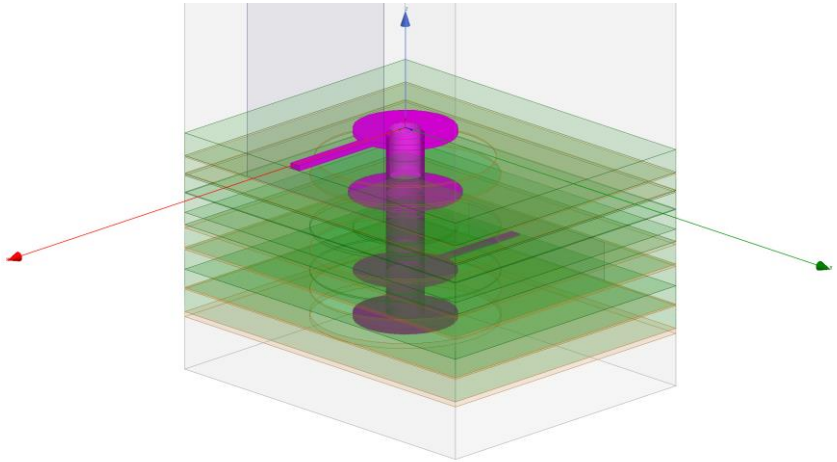
HDI Design rules: Classification

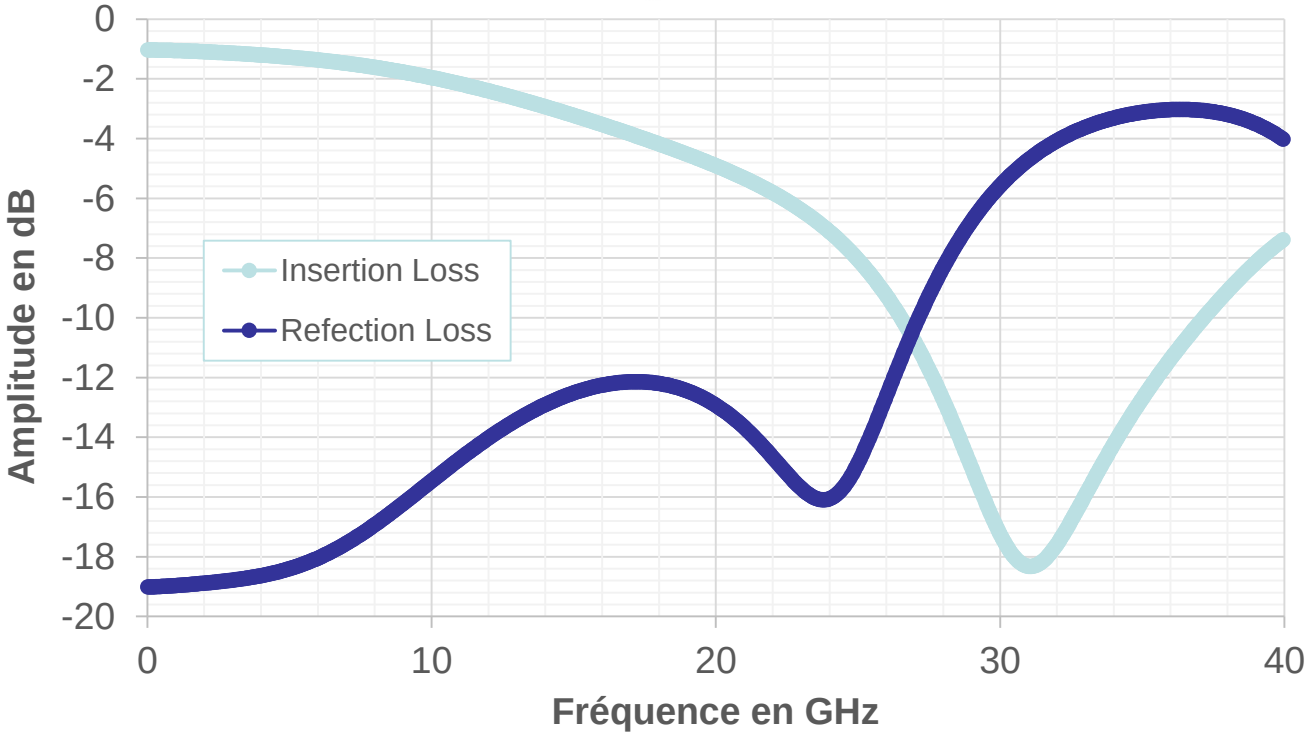


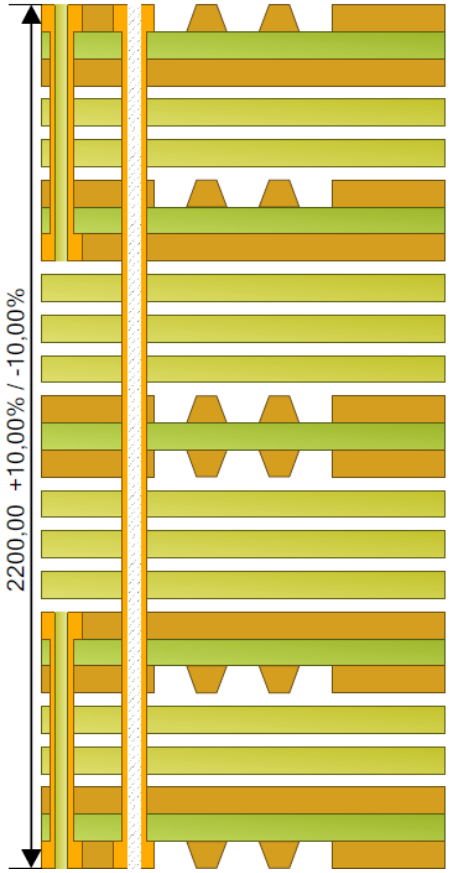
- Registration = difficult : LDI, Inkjet, … ?

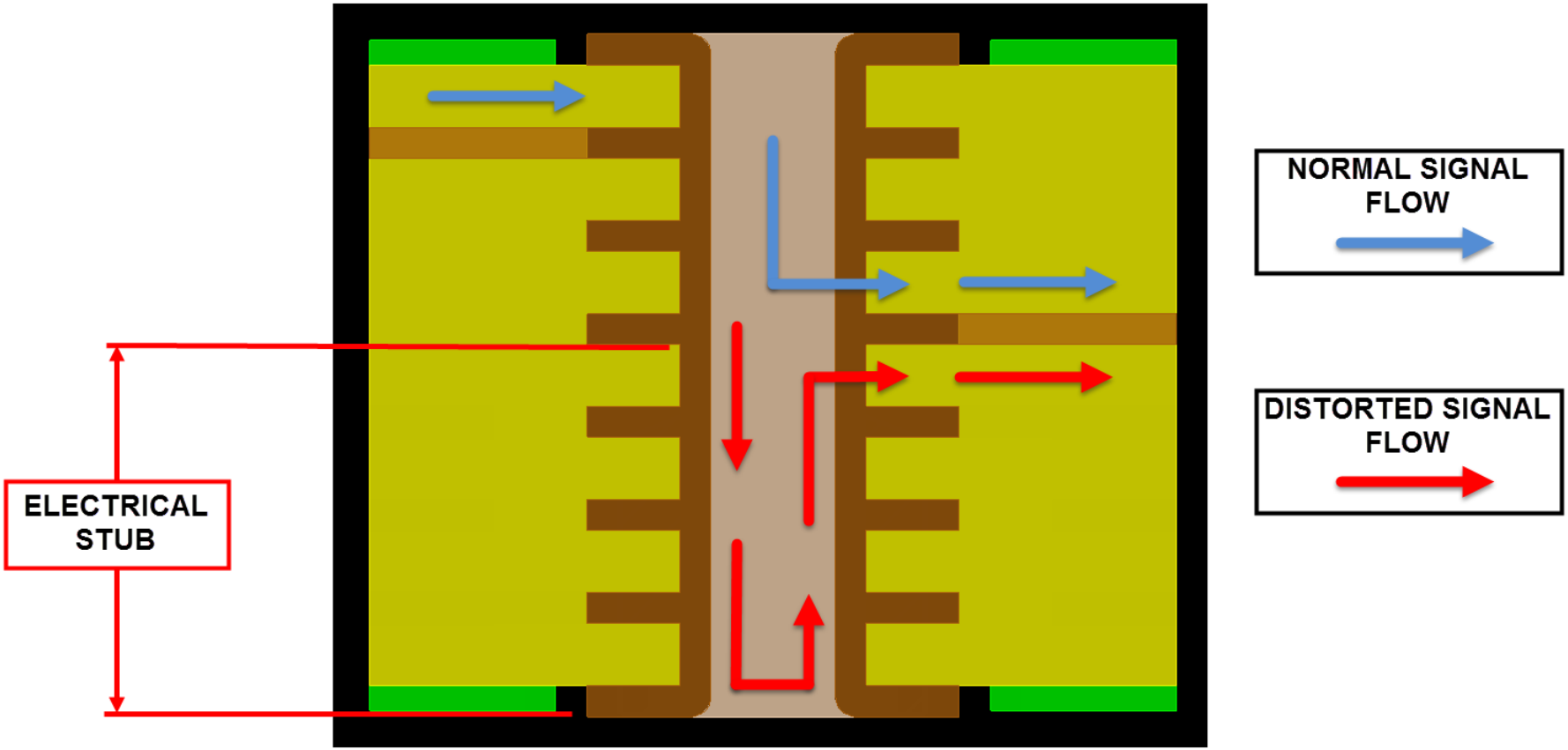


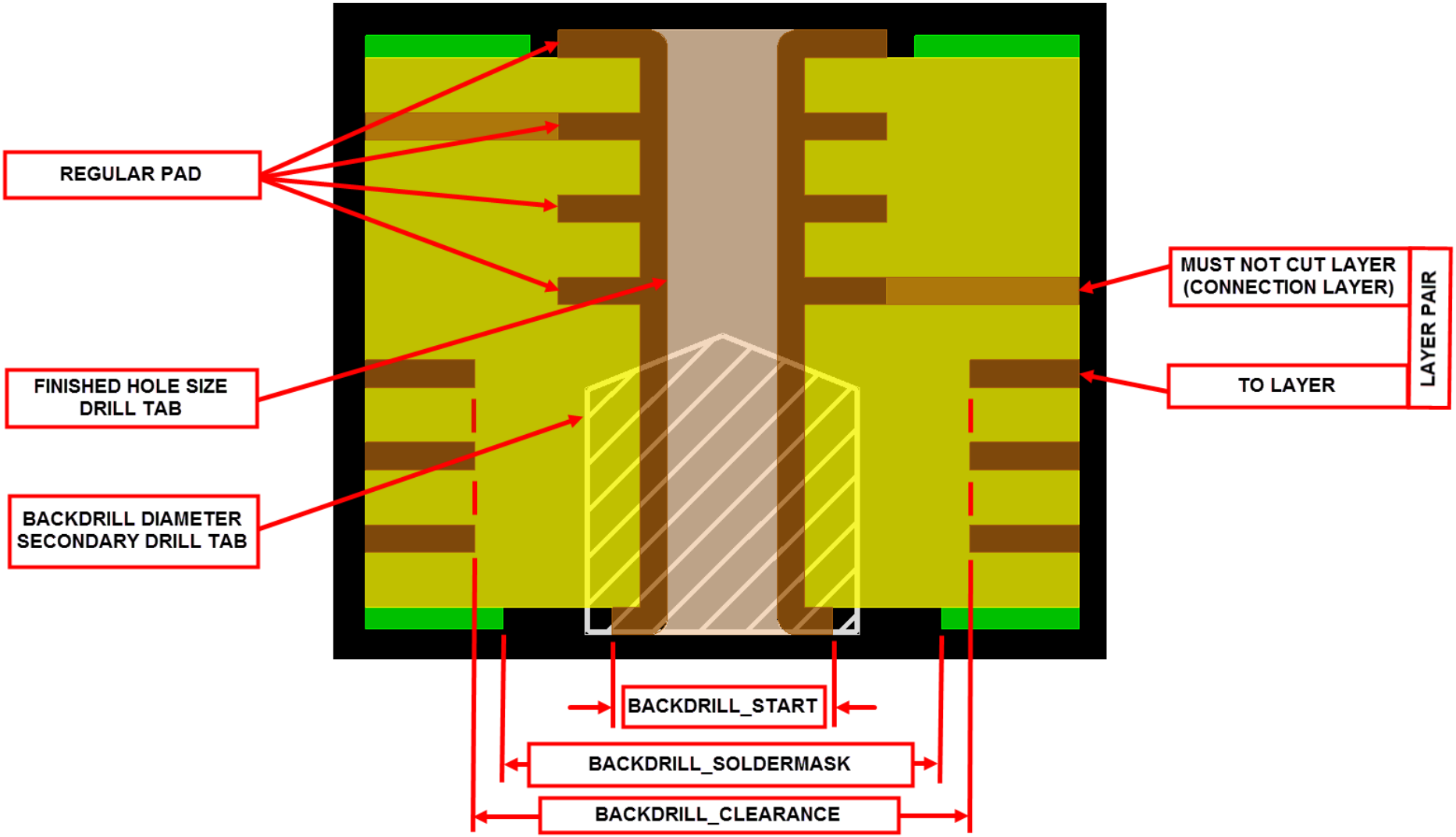
	Class					2008	2009	
	5	6	7	8	9	10	11	12
MAR & MOC : Typical	75	62.5	50	43.5	37.5	30	25	
MAR & MOC : Exceptional	50	43.5	37.5	30	25	25	25	
MSM	125	100	87	87	75	60	50	

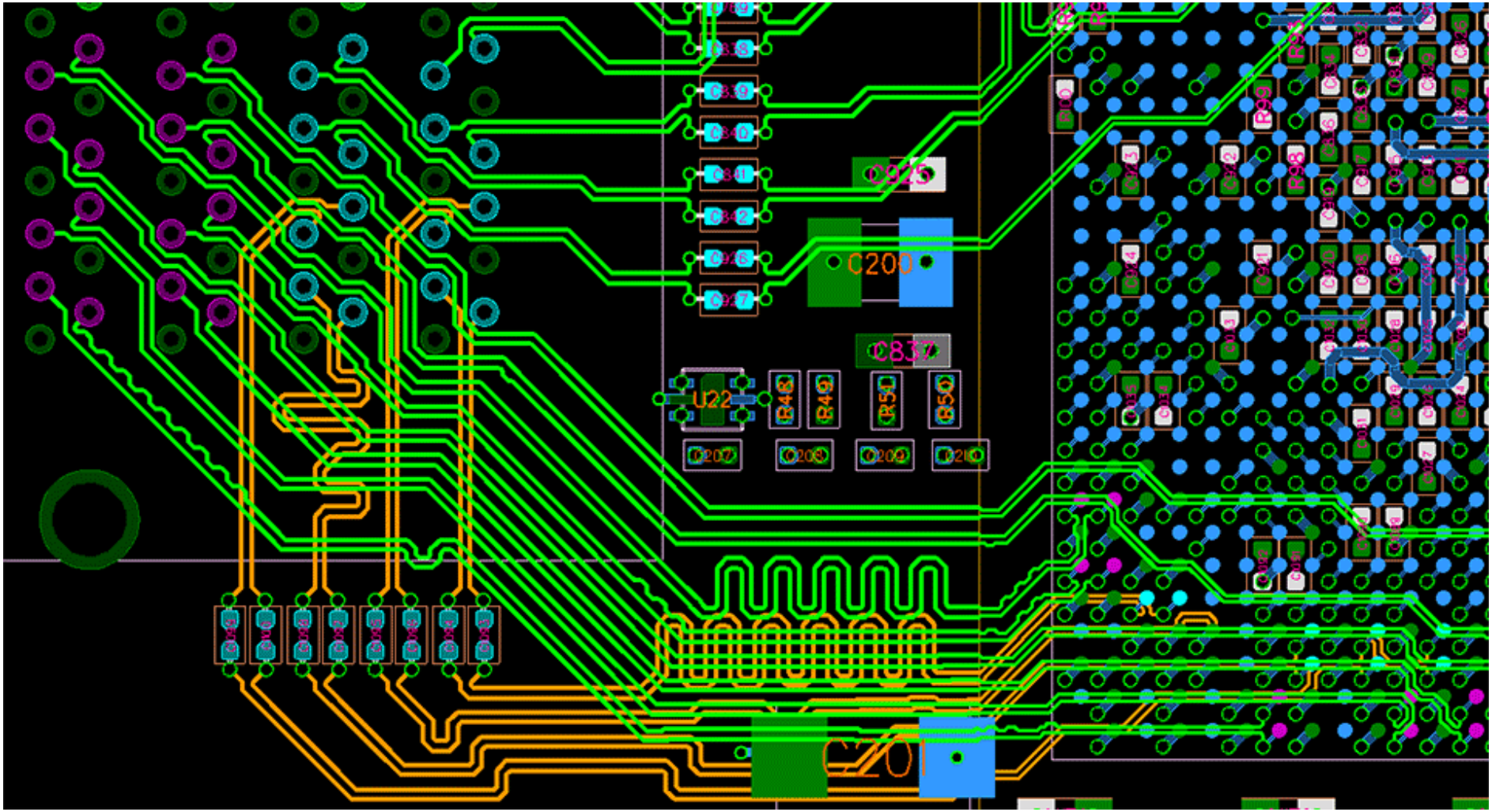


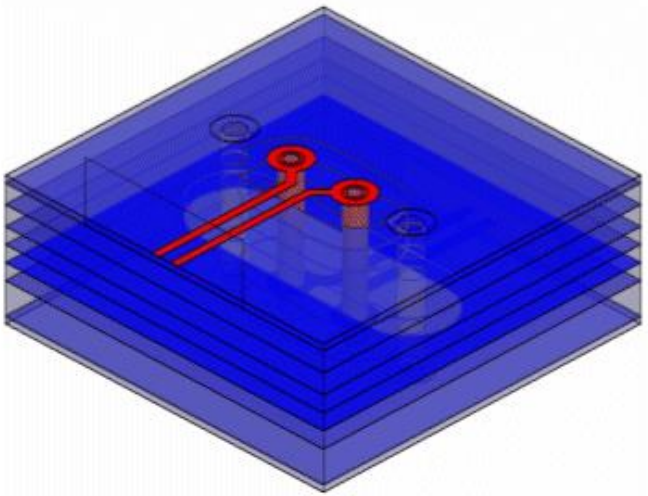

0
-2
-4
-6
-8
-10
-12
-14
-16
-18
-20
Amplitude en dB
Insertion Loss
Refection Loss
0
10
20
30
40
Fréquence en GHz

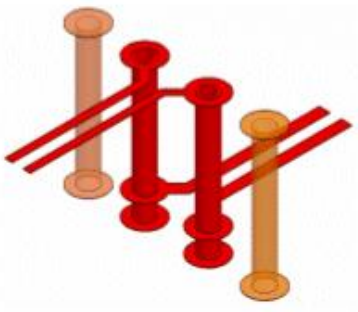

2200,00 +10,00% / -10,00%

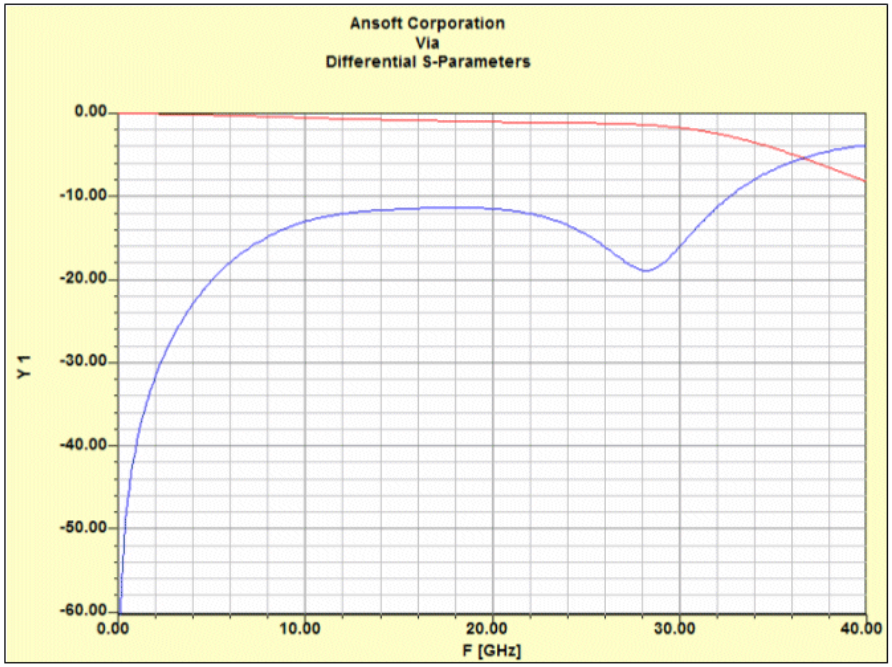

ELECTRICAL STUB
NORMAL SIGNAL FLOW
DISTORTED SIGNAL FLOW

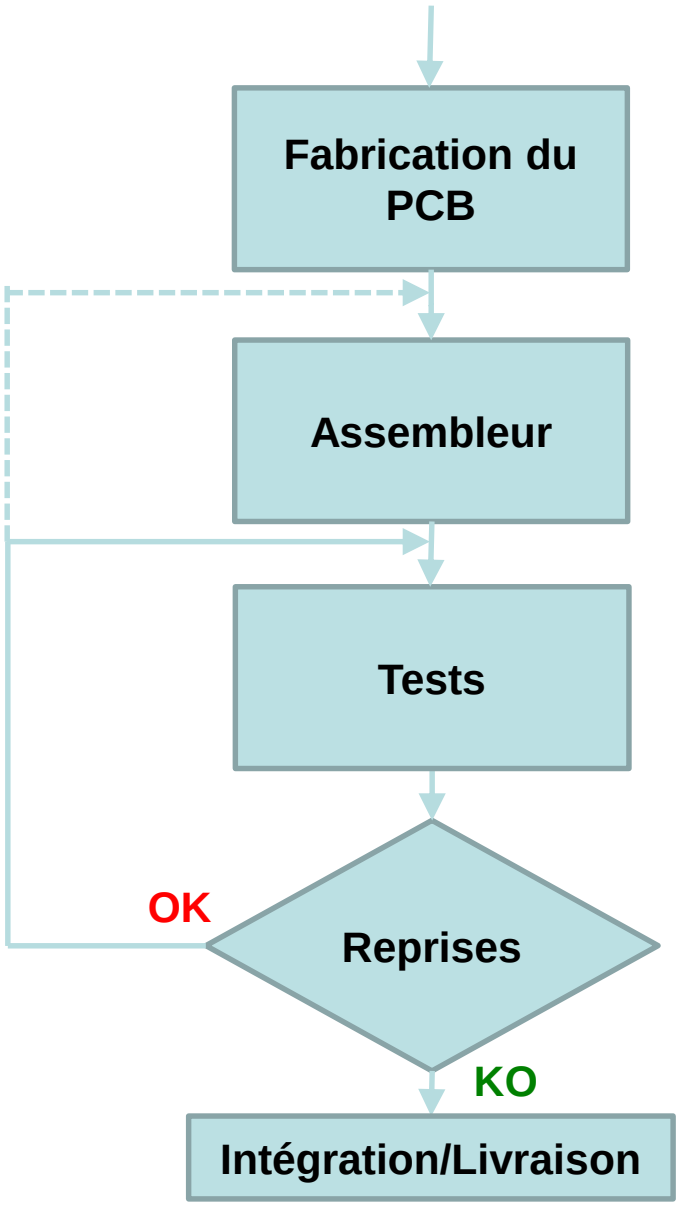

REGULAR PAD
FINISHED HOLE SIZE
DRILL TAB
BACKDRILL DIAMETER
SECONDARY DRILL TAB
MUST NOT CUT LAYER
(CONNECTION LAYER)
TO LAYER
LAYER PAIR
BACKDRILL_START
BACKDRILL_SOLDERMASK
BACKDRILL_CLEARANCE


C200
C201
U22
R46
R49
R50
R50






Ansoft Corporation
Via
Differential S-Parameters
0.00
-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
Y 1
0.00
10.00
20.00
30.00
40.00
F [GHz]



- Fichiers Gerber pour fabrication (couches + vernis + impression)
- Fichiers de perçage

- IPC-A-600
- Coupes métallographiques
- Fichiers gerber pour écrans (brasure)
- Repères topographiques
- Fichier Fabmaster
- Tests Takaya, Lit à clous
- Images RX

- IPC-A-610
- Tests électriques
- Tests fonctionnels
- Fiche de suivi
- Rapport de test

- **Nom des couches (IPC-D-350) : exemple d'un 12 couches**
  - Primary side (Top) : Layer 1
  - Couche interne 1 : Layer 2
  - Couche interne 2 : Layer 3
  - Couche interne 3 : Layer 4
  - Couche interne 4 : Layer 5
  - Couche interne 5 : Layer 6
  - Couche interne 6 : Layer 7
  - Couche interne 7 : Layer 8
  - Couche interne 8 : Layer 9
  - Couche interne 9 : Layer 10
  - Couche interne 10 : Layer 11
  - Secondary side (Bottom) : Layer 12
  - Vernis sur primary side : Layer 13
  - Vernis sur secondary side : Layer 14
  - Impression sur primary side : Layer 15
  - Impression sur secondary side : Layer 16

- **Gerber**
  - Un fichier par type de trou avec tableau (identifiant, quantité, diamètre fini, NPTH ou PTH)
    - Borgnes
    - Enterrés
    - Traversants

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
✱	19	14.00mil (0.356mm)	PTH	Round
✖	12	28.00mil (0.711mm)	PTH	Round
○	6	39.37mil (1.000mm)	PTH	Round
◘	14	40.00mil (1.016mm)	PTH	Round
▽	9	41.00mil (1.041mm)	PTH	Round
⌘	2	41.34mil (1.050mm)	PTH	Round
✡	6	60.00mil (1.524mm)	PTH	Round
⌑	11	64.96mil (1.650mm)	PTH	Round
✪	4	65.00mil (1.651mm)	PTH	Round
⊠	3	74.80mil (1.900mm)	PTH	Round
◇	18	100.00mil (2.540mm)	PTH	Round
◉	2	121.00mil (3.073mm)	PTH	Round
▼	18	130.00mil (3.302mm)	PTH	Round
	124 Total			

Drill Schedule

- **Excellon**
  - Contient les coordonnées des tous
  - Un fichier par type de trou

Inspection visuelle de la carte nue

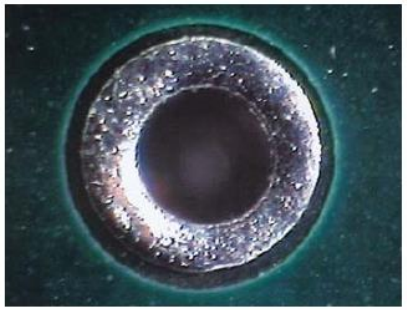


Figure 292a

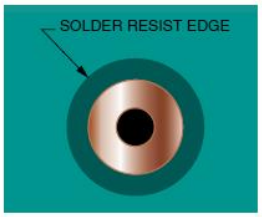


Figure 292b

Target Condition - Class 1, 2, 3

- No solder mask misregistration. The solder mask is centered around the lands within the nominal registration spacings.

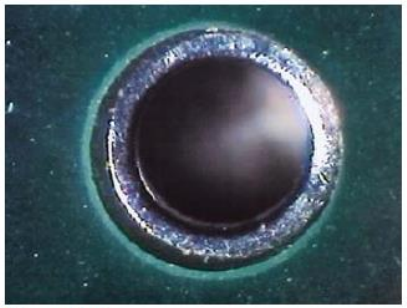


Figure 292c

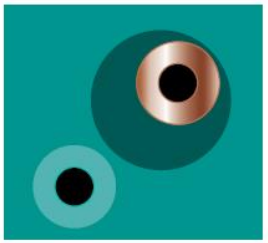


Figure 292d

Acceptable - Class 1, 2, 3

- Misregistration of the mask to the land patterns but the solder mask does not violate minimum annular ring requirements.
- No solder mask in PTHs, except those not intended for soldering.
- Adjacent, electrically isolated lands or conductors are not exposed.

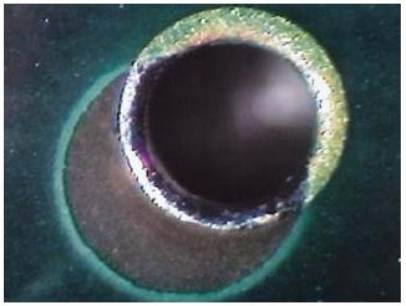


Figure 292e

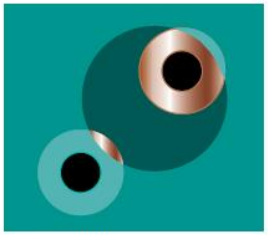
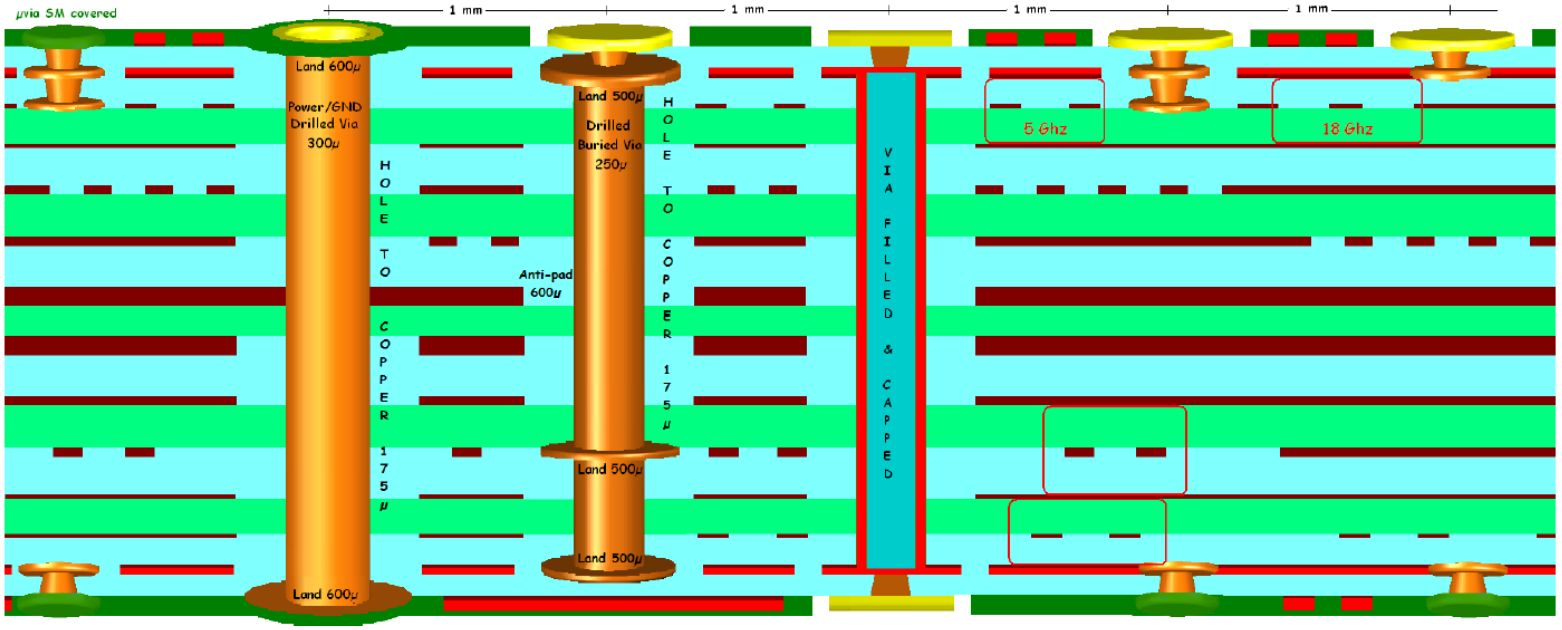


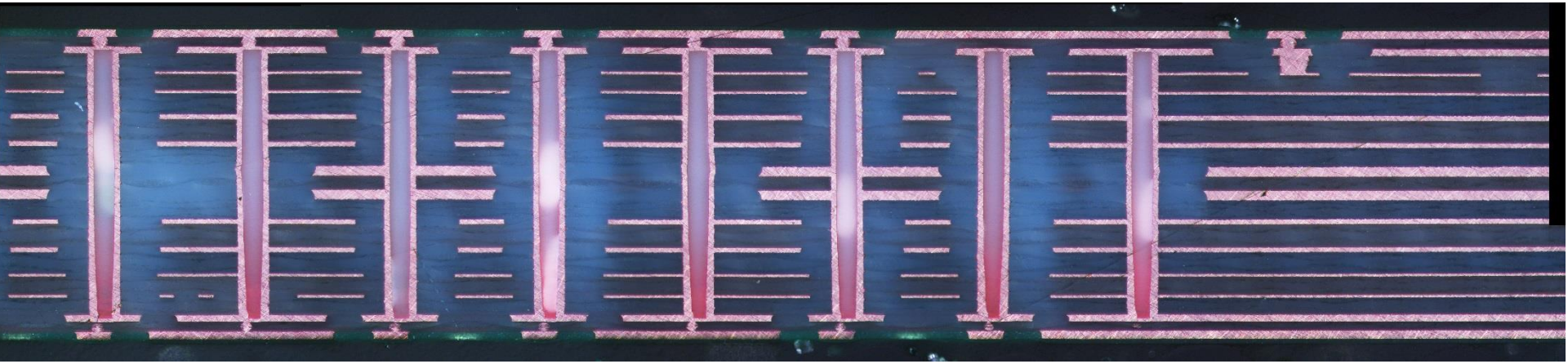
Figure 292f

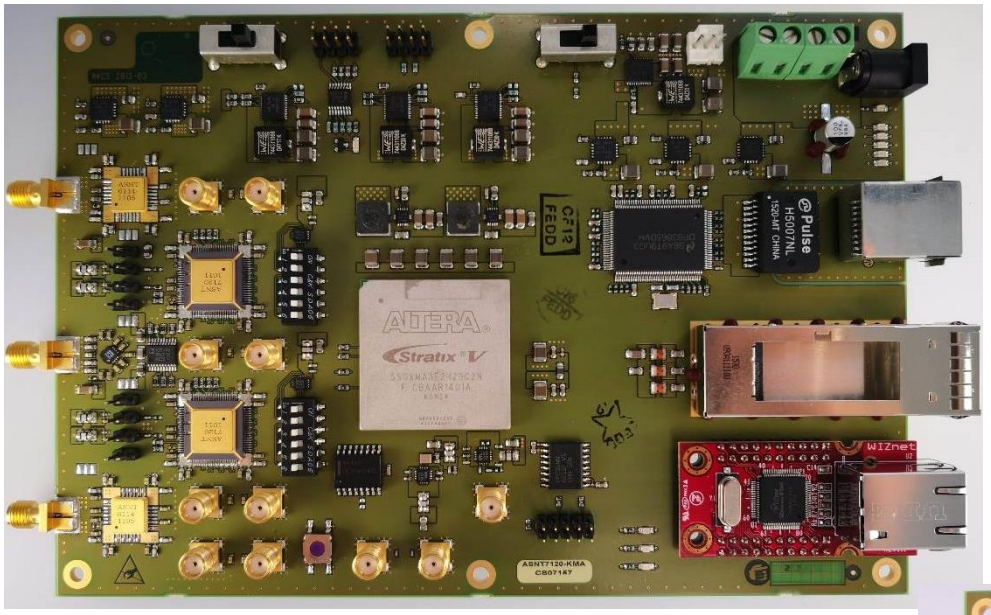
Nonconforming - Class 1, 2, 3

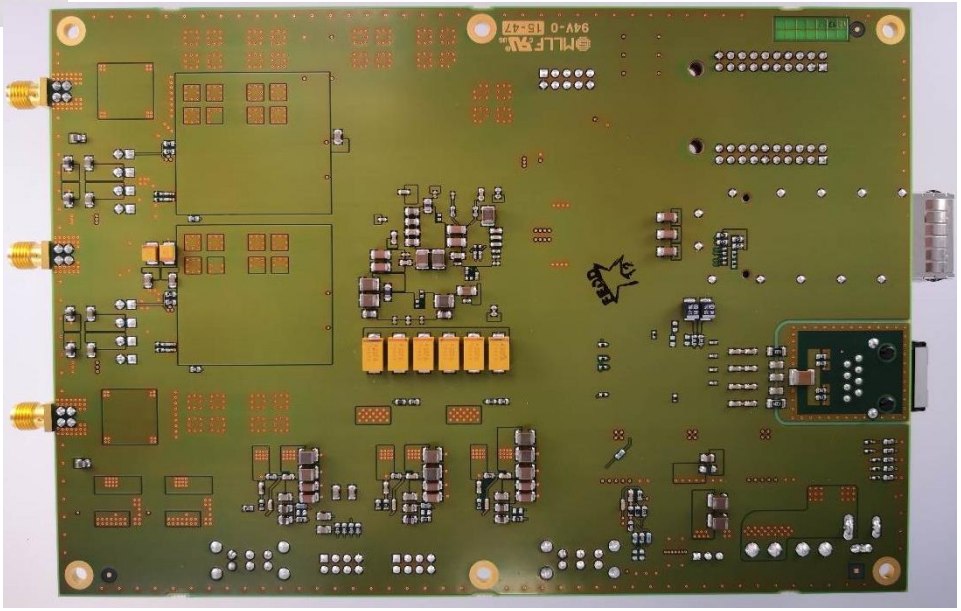
- Defects either do not meet or exceed above criteria.

Inspection visuelle des coupes métallographiques

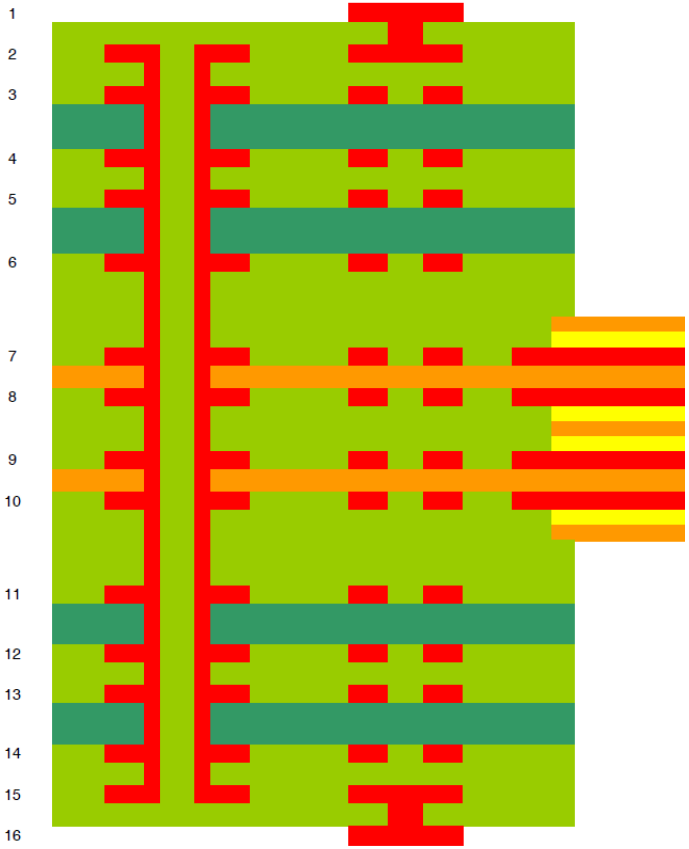


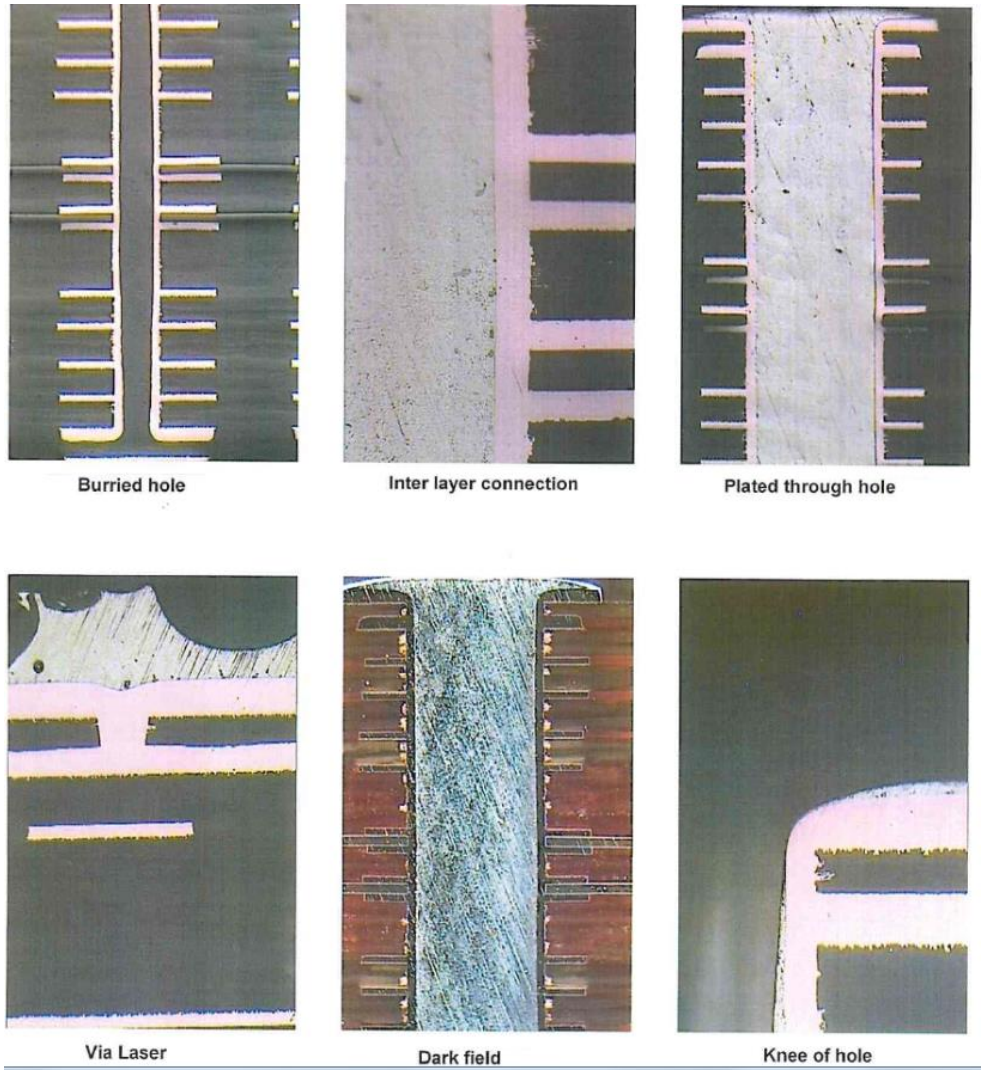



ALTERA
Stratix V
Pulse
H5007NL
WIZnet

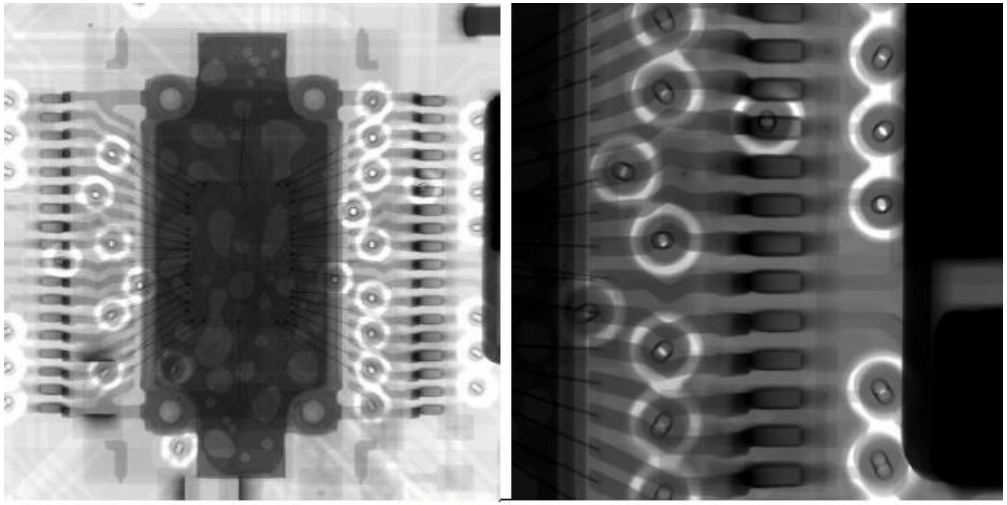


Inspection visuelle des coupes métallographiques

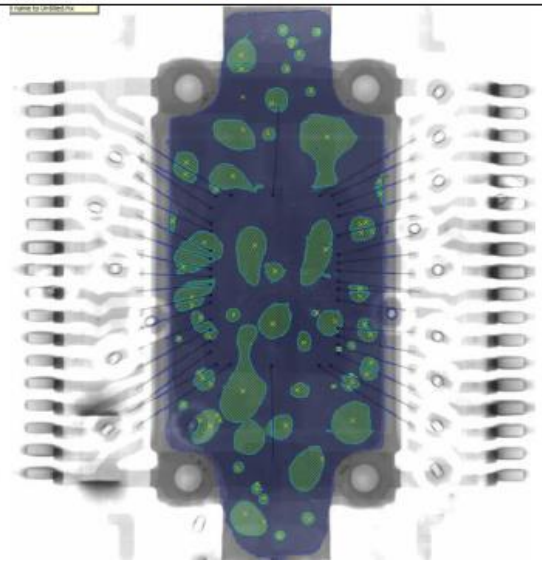


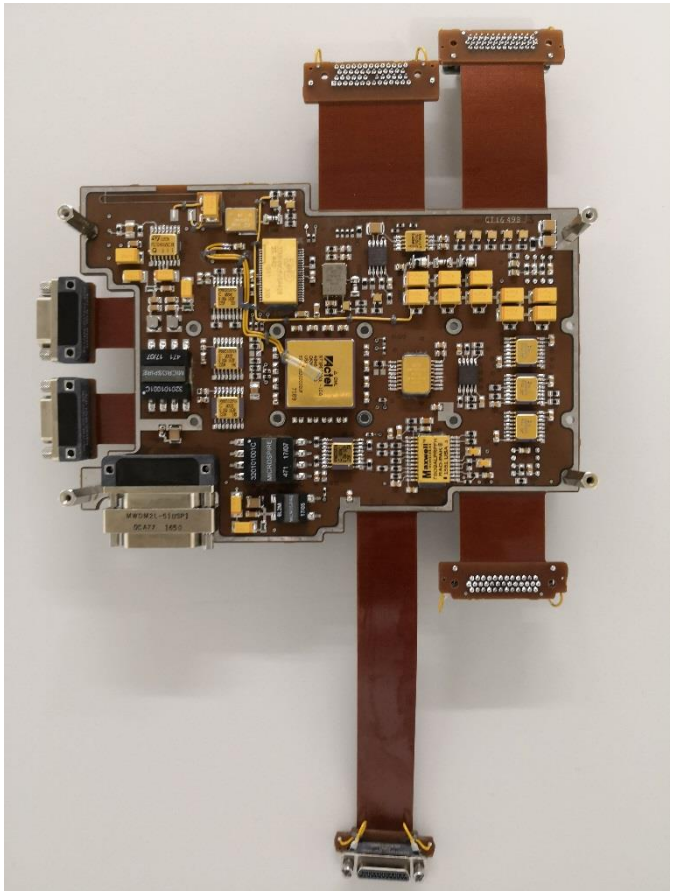


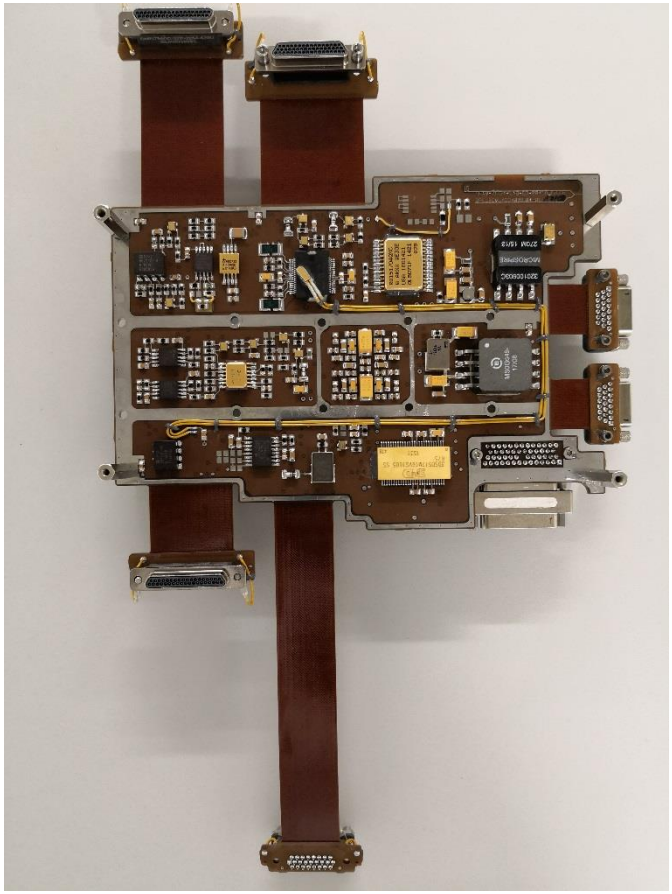
Contrôle des brasures sous composants

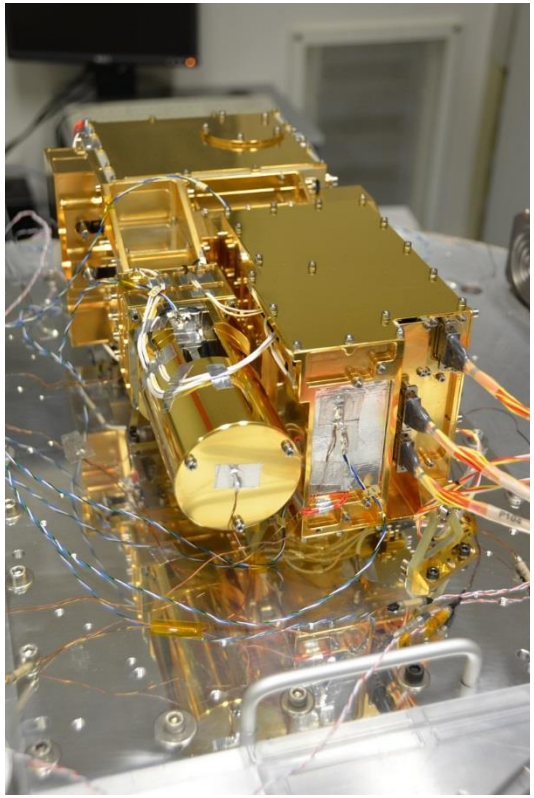


Rate of voids : ~ 25 %

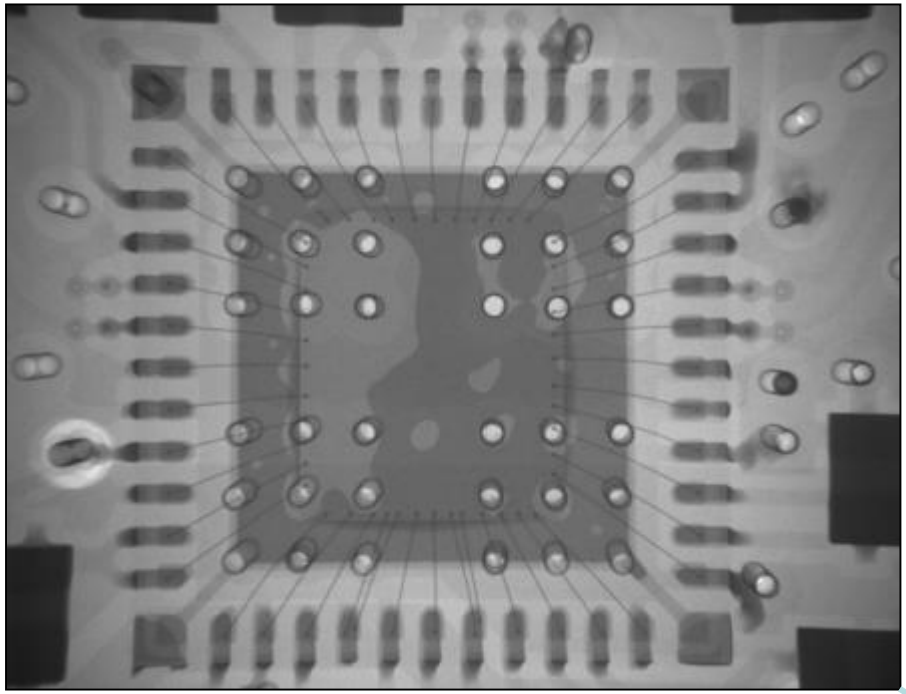


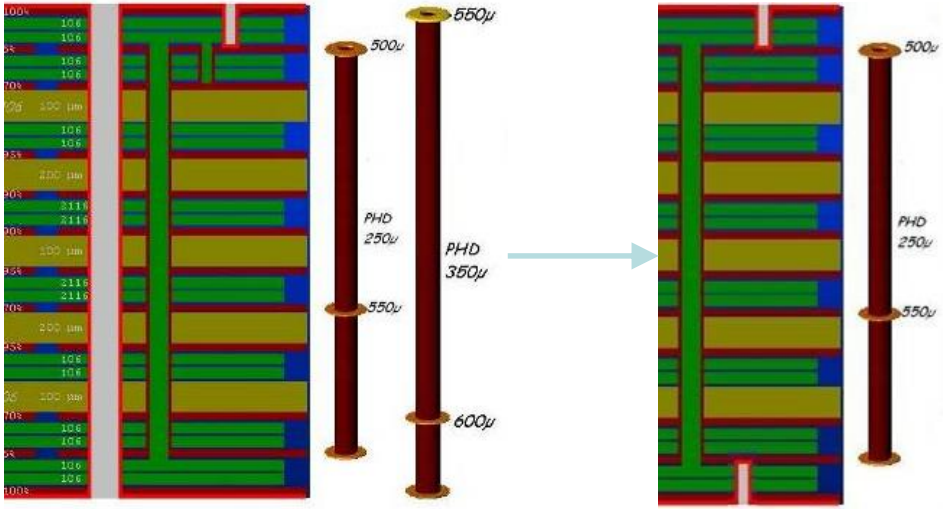


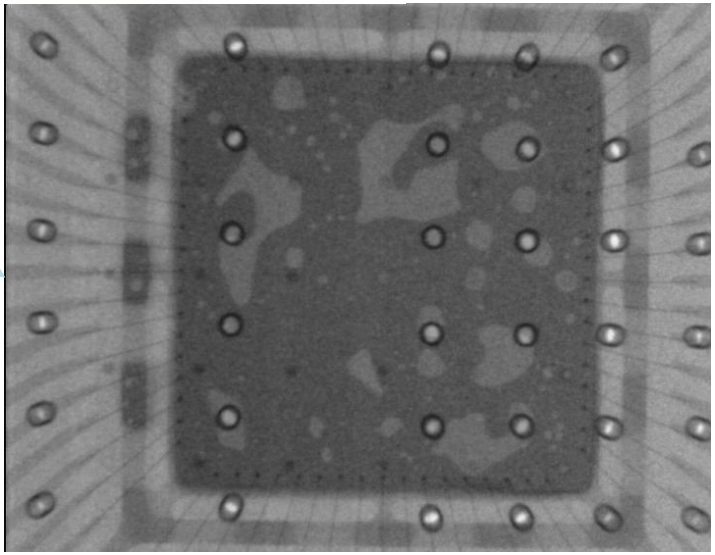


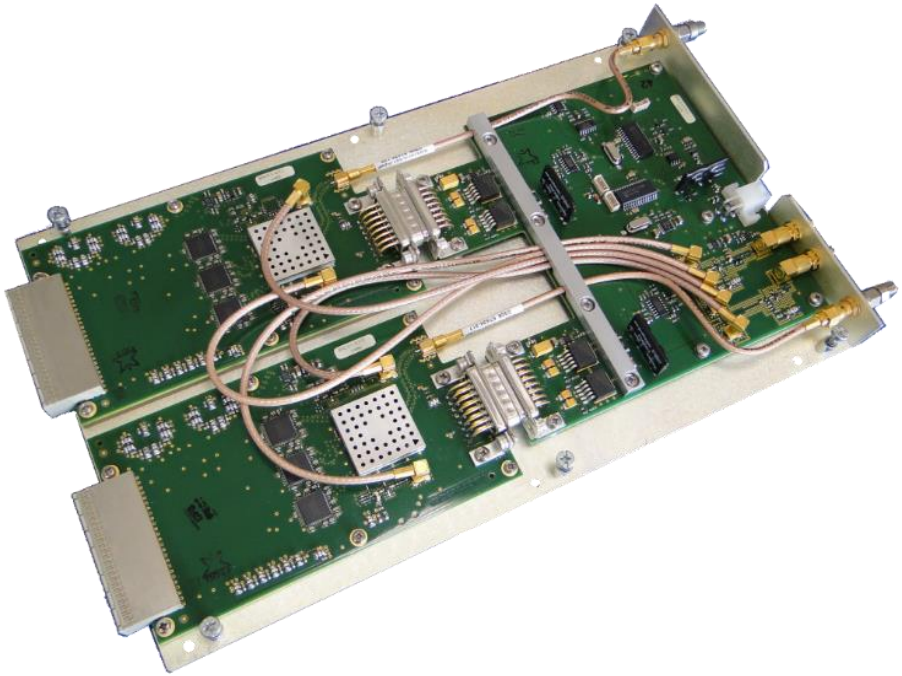


▪ Contrôle des brasures sous composants









Thank you!